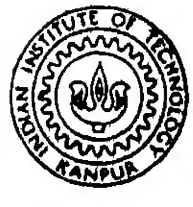
DESIGN AND IMPLEMENTATION OF A 140 MBPS MBIC CODER-DECODER AND A BIT SYNCHRONIZER

by

RAVI CHANDRAN K



DEPARTMENT OF ELECTRICAL ENGINEERING

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DESIGN AND IMPLEMENTATION OF A 140 MBPS MB1C CODER-DECODER AND A BIT SYNCHRONIZER

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CERTIFICATE

It is certified that the work contained in the thesis entitled Design and implementation of a 140 Mbps mB1C coder-decoder and a bit synchronizer', by Ravi Chandran K, has been carried out under our supervision and that this work has not been submitted elsewhere for a degree

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Ravi Chandran K

ABSTRACT

An mB1C coder-decoder circuit is designed and implemented for use in high speed fiber optic digital communication systems mB1C is a line coding technique, normally used at frequencies beyond 100 Mbps, to overcome the effects of the base line wander, while introducing BSI (Bit Sequence Independence) conditions BSI conditions include the requirements that the timing information should be extractable from any received bit sequence, and in-service error monitoring should be possible at the decoder

To extract the timing information, a bit synchronizer is used By nonlinear processing of the input NRZ (non-return to zero) data, a discrete spectral component is regenerated at the data rate A delay and Ex-OR type of nonlinearity has been used to generate this discrete spectral component The output of the nonlinear circuit is then filtered through a PLL and the desired clock is regenerated for use in the decision circuit of the receiver

The coder-decoder and the bit synchronizer circuits are tested and found to work satisfactorily till 100 Mbps, beyond which interference and attenuation of signals set in Suggestions for the improvement of the data rate are given at the end of the thesis

LIST OF FIGURES

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CHAPTER 1

INTRODUCTION

1.1 INTRODUCTION

Great interest in communicating at optical frequencies was generated in 1960 with the advent of the laser, which made available a coherent optical source The development and application of optical fiber systems grew from the combination of the semiconductor technology, which provided the necessary light sources and photo detectors, and the optical wave guide technology

The primary advantage of optical fiber is the large bandwidth that it offers Since the carrier is an optical signal with a frequency exceeding 10^{14} Hz, it is conceivable that bandwidths of the order of 10^{4} GHz can be supported The inherent advantage of optical fiber communication over conventional copper system include the following

1 low transmission loss and wide bandwidth,
2 small size and weight,
3 immunity to interference,
4 electrical isolation,
5 signal security, and
6 abundance in the availability of raw material

In view of these advantages of optical fiber systems, they are expected to find enormous application potential in a number of areas of communications Some of the important areas where such systems are likely to find immediate applications are in military, telecommunication systems, computer to computer links, biomedical instrumentations in integrated optical devices, etc Digital communication techniques are mainly followed for optical fiber communication systems

1 2 DIGITAL FIBER OPTIC COMMUNICATION SYSTEM

The block diagram of a typical fiber optic digital communication system [1,2,3] is shown in Fig 1 1 The binary input digital data is suitably coded by an encoder The coded electrical data pulses are now converted into corresponding optical pulses by either an LED or a Laser

These optical pulses propagate through the glass fiber and are detected by a photodetector A PIN photodetector or an avalanche photodetector (APD) is commonly used The process of detection results in the generation of signal dependent shot noise An amplifier, with a low noise front end (preamplifier), amplifies the photo detected current High impedance (HZ) or Transimpedence (TZ) preamplifier are the possible configurations TZ amplifiers are preferred, since they often eliminate the need for equalization

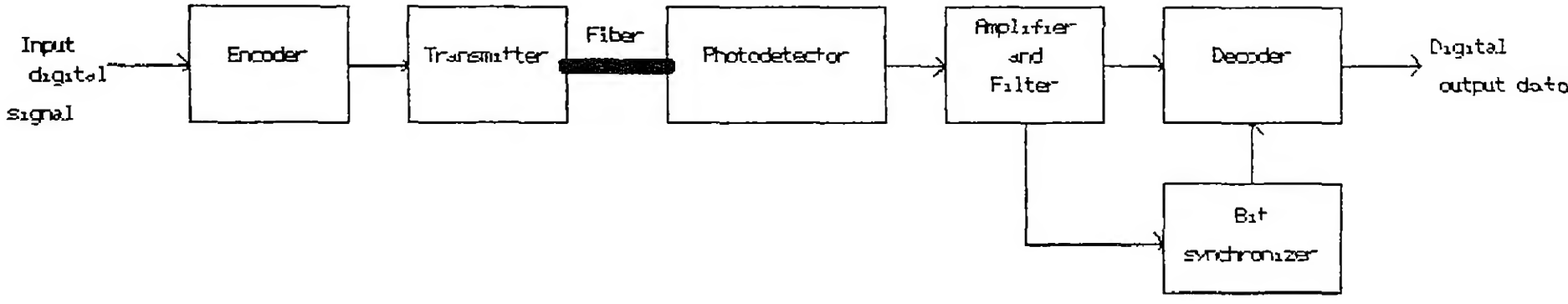


Fig.1 1 Block diagram of a digital optical fiber communication system

In general, for PIN photodiodes, the thermal noise currents of the detector load resistor and the active elements of the amplifier circuitry are the dominant noise sources For avalanche photo diodes the thermal noise is of lesser importance and the photodetector noises usually dominate

The equalizer that follows the amplifier is normally a linear frequency shaping filter that is used to mitigate the effects of signal distortion and inter symbol interference (ISI) The recovered signal is used by the bit synchronizer for clock recovery, which is then used by the decoder for retrieving the original data

1 3 LINE CODING

In designing digital transmission systems, one of the most important problems is the choice of a suitable line code A digital transmission system should have a transmission capability with Bit-Sequence-Independence (BSI) [4,5,6] BSI conditions include the requirements that

1 timing information can be extracted from any information sequence, and
2 false synchronization does not occur

Conditions also desirable for a line code are

3 no error increase occurs during encoding and decoding,

4 DC base line fluctuations of the pulse stream should be negligible,

5 in-service error monitoring at terminals be possible, and

6 code converter construction should be simple

Additionally, suppression of the bit rate increase is important in high speed digital transmission systems, because an increase in transmission speed adds to the difficulties in realizing electronic circuits

Line codes such as mBnB satisfying BSI conditions are already being used as the line code for optical fiber transmission systems having a low bit rate However, these codes are hardly applicable for high bit rate systems, because it is difficult to build transmission equipment for these codes at high data rates This is so because it is not possible to obtain sophisticated electronic circuits for mBnB code conversion at high bit rates In our work, mB1C code [7] is used as a new line code for high speed transmission In mB1C code we have m binary bits with one complement bit insertion More on mB1C codes is given in Chapter 2

1.4 SYNCHRONIZATION

Synchronization, as required in the context of modern digital communication systems, consists of estimating two parameters

of the received signal, frequency and time [8,9,10] In the implementation of a modern digital communication system, several levels of synchronization are necessary

The following types of synchronization are used in modern digital communication systems [11]

1 carrier synchronization,

2 clock or bit synchronization,

3 code word or node synchronization,

4 frame or word synchronization, and

5 network synchronization

Bit synchronizer and word synchronizer are used in the coder circuit designed in this work

1.4.1 BIT SYNCHRONIZATION

Optimum detection of the data requires a local clock generator that is in close phase agreement with the received pulse train Two factors have to be considered while designing digital communication systems requiring bit synchronization First, it is necessary to maintain high efficiency in the data detection process for accurate synchronization Inaccurate synchronization reduces the probability of making correct decisions Secondly, from the given amount of power available for transmission, the synchronization scheme should require as little of this as possible

Thus, a conflict exists between establishing a good symbol synchronization and the one with the requirement of minimum energy

The data itself is used for regeneration of clock in most digital communication systems This technique is called the data derived bit synchronization Digital communication systems that are efficient in power requirements and bandwidth occupancy, mainly transmit signal pulses in the NRZ (non-return to zero) pulse formats

The spectrum of the NRZ data does not contain a discrete spectral line at the data rate The problem of synchronization is simplified in the case of RZ (return to zero) pulse formats as they have a discrete frequency component at the clock frequency It is a simple process to convert the NRZ data to the RZ format, i e , by Ex-ORing with its own delayed version Obviously, the duration of the delay should be less than one data period

A PLL (phase locked loop) or a tuned circuit is used to extract the spectral component at the data rate The extracted signal is used by a pulse generator to generate the timing waveform [12] The variance of the output jitter has been shown to consist of three parts due to thermal, shot, and pattern noise This variance is reduced by decreasing the loop bandwidth In the synchronizer developed, we have used a PLL

1 4 2 WORD SYNCHRONIZATION

The input data to be transmitted is broken into words of four bit lengths each Line coding is done with these words of data At the decoder, it is necessary that the blocks are separated correctly for proper decoding The property of mB1C codes, whereby the $(m+1)^{th}$ bit is the complement of the m^{th} bit is used for word synchronization By Ex-ORing the m^{th} and the $(m+1)^{th}$ bit, the error signal is generated and is used for word synchronization This can also be used for error monitoring

1 5 SCOPE OF THE PRESENT WORK

In the present work, mB1C coder and decoder circuits are realised Our aim is to achieve the maximum frequency possible with the available haidware In the coder circuit, m bit data blocks are converted into m+1 bits each We have two clock signals, the coder clock (f_{cc}) to clock the uncoded data and the line clock (f_{lc}) to clock the coded data A PLL frequency synthesizer is used to generate the line clock f_{lc} from the coder clock f_{cc}, such that $f_{cc}/m = f_{lc}/(m+1)$ In the decoder, m+1 coded bits are converted into m decoded bit blocks Here the line clock in decoder f_{ld} is used to clock the coded data recievied and decoder clock f_{cd} to clock the decoded bits The decoder clock f_{cd} is generated from the line olock using a frequency synthesizer PLL, such that $f_{ld}/(m+1)$ =

fcd/m The line clock itself is generated using another type of PLL which is popularly known as bit synchronizer Here the line clock is derived from the coded data received from the coder The bit synchronizer designed in this work is of the delay and EX-OR type We have also used a word synchronizer to provide the correct block of coded data for the decoder By analyzing the timing diagram of the coder and the decoder circuits, it is established that the circuits are capable of working beyond 140 Mbits per second

1 6 THESIS OUTLINE

This thesis comprises five chapters Chapter 2 gives an overview of the different types of line coding used in optical fiber communication systems The power spectral density of mB1C code is derived and its importance is specified for high frequency optical fiber communication systems Chapter 3 describes the coder circuit implemented in this work It gives the timing diagram for the coder circuit, from which the maximum frequency up to which the circuit will be capable of operating is calculated The PLL used for synchronization of the two clocks used in the coder circuit is also described Chapter 4 describes the decoder circuit and its timing diagram The bit synchronizer used for retrieving the clock from the data at the receiver is described here Chapter 5 gives the summary and conclusion with a discussion on the results and some suggestions for possible future work

CHAPTER 2

LINE CODING

2.1 INTRODUCTION

In designing any digital transmission system, one of the most important problems is the selection of the best suitable line code In this chapter, the importance and the various types of line codes are discussed Finally, the advantages of the mB1C code are illustrated

2 2 LINE CODING FOR OPTICAL FIBER COMMUNICATION

In any digital optical fiber data link, the decision circuitry in the receiver must provide precise timing information extracted from the incoming optical signal False synchronization should not occur Since errors resulting from channel noise and distortion mechanisms can distort the signal, it may be desirable for the optical signal to have an inherent error deteotion capability These features [4] can be added into the raw data stream by encoding the signal by adding extra bits Signal encoding uses a set of rules for arranging the signal symbols in a particular pattern This process is called as transmission or line coding

Binary codes are widely used as transmission line codes in

optical digital transmission systems This is because of the nonlinear nature of the light sources, i e , the intensity of the light output from the light sources used, varying nonlinearly with the modulating current Therefore, the decision levels would require to be nonuniformly spaced in a multi level system This complicates the receiver and the transmitter drive circuits Several kinds of binary codes have been proposed, such as

1 two level AMI (Alternate Mark Inversion) codes [13],
2 mBnB codes [14], and
3 mB1C codes [7]

2 3 AMI CODES

The AMI (Alternate Mark Inversion) codes were originally bipolar They are called AMI because the polarities of the marks (high level) are inverted alternately It contains little low frequency component, hence, ac-coupled amplifiers have no base line wander Pulse errors can also be detected by examining the AMI rule violation in a pulse train

For optical fiber communication, two types of unipolar AMI codes are used as shown in Fig 2 1 They are

1 CMI (Coded Mark Inversion) code, and
2 DMI (Differential Mark Inversion) code

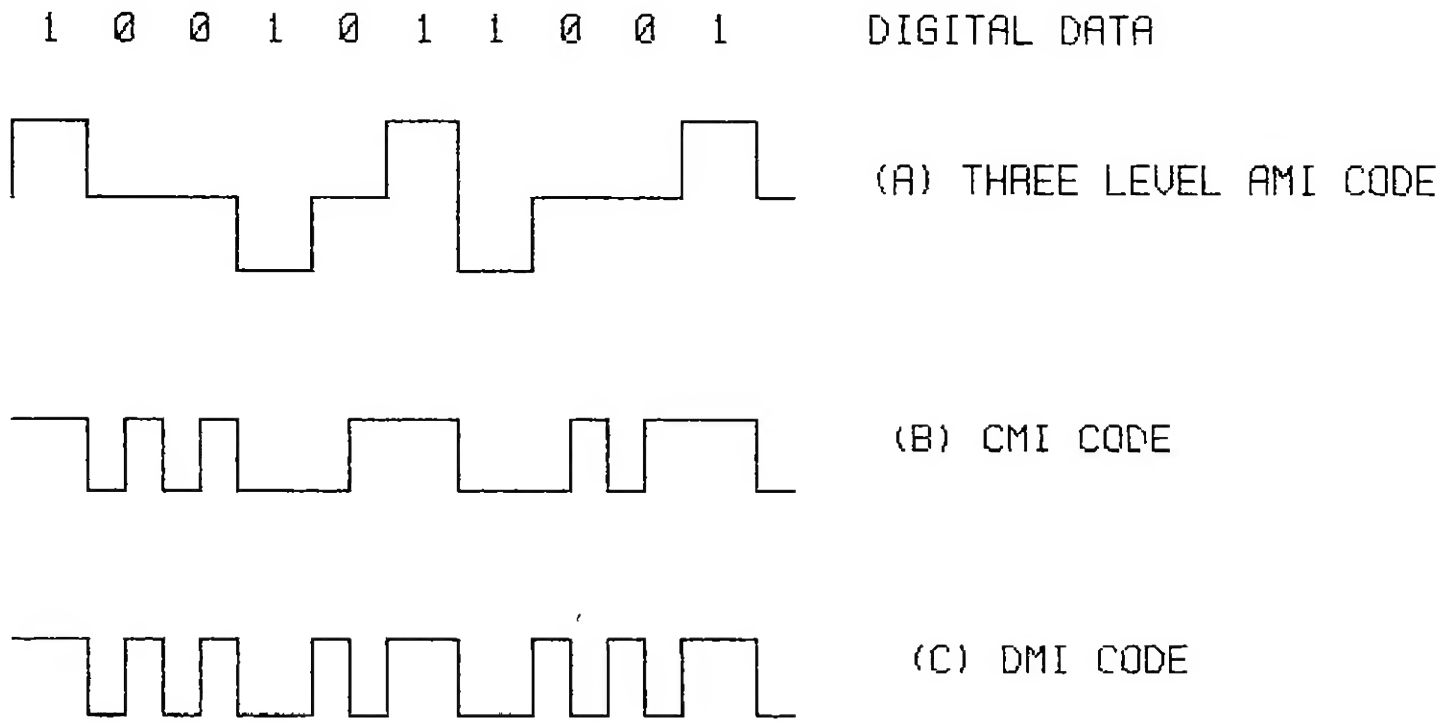


Fig.2.1 AMI codes.

In CMI codes, the mark (high level) is represented as a (1,1) or a (0,0) alternately The space (low level) is represented by a (0,1) always In DMI codes, the mark (high level) is again represented as a (1,1) or a(0,0) The space (low level) is represented either by a (0,1) or by a (1,0) such that the first bit is complement of its preceding bit

CMI and DMI codes contain only a small number of maximum consecutive identical digits (3 and 2 respectively) They poses a good balance of ones and zeros, i e , they have a low DSV (Digital Sum Variance) These code converters can be easily made However, these codes are not suitable for high bit rate systems since they require a bit rate which is, twice as much as the information bit rate

2.4 mBnB CODES

In mBnB block codes, the data is separated into blocks, each having m bits These blocks are converted into blocks of n bits before transmission, where n is greater than m The conversion is made using a table which has to be designed to achieve the required objectives The two level AMI format can be considered to be an mBnB coding plan that converts one bit into two bits (1B2B code)

2.4.1 PROPERTIES OF mBnB CODES

1 The efficiency η of an mBnB code gives a measure of how many extra bits are added to achieve the objectives of line coding and is given by

$$\eta = (m/n) \tag{2.1}$$

2 The transmitted symbol period is given by

$$T_{mn} = T_{ii}\ \eta, \tag{2.2}$$

where T_{ii} is the period of 100% efficient code

3 Increase in the transmitted bandwidth and the data rate is given by

$$(n/m) = (1/\eta) \tag{2.3}$$

4 The dispersion factor α is

$$\alpha_{mn} = (\alpha_{ii}/\eta), \tag{2.4}$$

where α_{ii} is the dispersion factor for 100% efficient codes

The dispersion factor α gives a measure of the increase in dispersion induced signal distortion Light pulse broadens as it travels along the fiber which eventually causes a pulse it to overlap with its neighboring pulses After a certain amount of overlap, adjacent pulses can no longer be individually distinguished at the receiver, and error will occur Smaller the efficiency, larger is the dispersion and, hence, its effects A comparison of several mBnB codes is given in Table 2.1

TABLE 2 1

A comparison of several mBnB codes

CODE	(n/m)	Nmax	D	W %
3B4B	1 33	4	±3	25
4B5B	1 25	5	±3	50
5B6B	1 2	6	±4	28
6B8B	1 33	6	±3	75
7B8B	1 14	8	±7	27
9B10B	1 11	11	±8	24

The parameters shown in this table are

1 *The ratio n/m which shows the bandwidth increase*

2 The longest number Nmax of consecutive identical symbols

3 The bounds on the accumulated disparity D Accumulated disparity gives the number of ones minus the number of zeros in a coded block

4 The percentage W of n-bit words that are not used The detection of words, which do not satisfy the coding rules, permits character reframing and error detection

The efficiency of mBnB codes improves with increasing m With the *increase in m, the number of signal transitions decreases,*

and consequently, the code becomes poorer in timing content The error multiplication also increases with increase in the value of m For each bit of error received, the whole block is in error and, hence, the receiver error spread is m bits per bit of received error Coding complexity increases with increase in the value of m As frequency is increased, it becomes very difficult to realize mBnB codes, because of the hardware complexities involved [9,15]

2.5 mB1C CODE

A new line code which satisfies all BSI (Binary Sequence Independence) conditions is realized by designing an additional bit after every m input bits This inserted bit is named a C (complement) bit and it is the complement of the m^{th} bit This coding format is called an mB1C (m binary with one complement bit insertion) code [7]

When the C bit and the succeeding m bits are identical, we have the maximum number of consecutive identical elements in an mB1C code Hence, the maximum number of consecutive identical bits N_{max} is equal to m+1 This code can be made more efficient by choosing higher value of m The upper value of m is restricted by the allowed limit of ISI (Inter Symbol Interference), since larger the number of consecutive identical digits, the more is the ISI

2.5.1 POWER SPECTRUM

When the input mark probability is 1/2, a discrete component is found at dc. When the input mark probability deviates from 1/2, discrete harmonic spectra which have a fundamental component of $1/((m+1)T_o)$ (where T_o is the code symbol period) are generated. The derivation of the continuous power spectrum for an mB1C code is given as follows.

The inclusion of C bit in mB1C codes introduces a degree of correlation into the coded signal process, and so renders the output spectrum nonwhite. Since the block coded signal processes are generally cyclostationary, recourse to phase randomizing or an equivalent averaging operation is required to obtain the spectrum [16, 17].

Let Y(n) denote the phase randomized discrete sequence corresponding to the cyclostationary coded sequence X(n). Let X(n) take the values +0.5 and -0.5 with equal probabilities.

The autocorrelation function of interest is

$$R_{yy}(j) \triangleq E\{Y(n)\ Y(n+j)\}, \qquad (2.5)$$

where E{ } denotes the expectation operator, and independence of n results from the phase randomizing operation. Thus, it suffices to

carry out the computation over a block of m+1 digits for X(n) Hence

$$R_{yy}(0) = \left[1/(m+1)\right] \sum_{n=1}^{m+1} \left\{P[X(n)=0\ 5](0\ 5)^2 + P[X(n)=-0\ 5](-0\ 5)^2\right\}, \tag{2 6}$$

$$R_{yy}(0) = 1/4, \tag{2 7}$$

similarly,

$$R_{yy}(J) = R_{yy}(-J) = \left[1/(m+1)\right] \sum_{n=1}^{m+1} \left\{P[X(n-J)=0\ 5](0\ 5)\ x\right.$$

$$P\left[X(n)=0\ 5 \mid_{X(n-J)=0\ 5}\right](0\ 5)$$

$$+ P[X(n-J) = 0\ 5](0\ 5)P\left[X(n)=-0\ 5 \mid_{X(n-J)=0\ 5}\right](-0\ 5)$$

$$+ P[X(n-J) = -0\ 5](-0\ 5)P\left[X(n)=0\ 5 \mid_{X(n-J)=-0\ 5}\right](0\ 5)$$

$$\left. + P[X(n-J) = -0\ 5]\ (-0\ 5)\ P\left[X(n)=-0\ 5 \mid_{X(n-J)=-0\ 5}\right](-0\ 5)\right\} \tag{2 8}$$

Considering the structure of mB1C codes in which the first m bits in each block are independent with P[X = 0 5] = P[X=-0 5] =

1/2, while the $(m+1)^{th}$ bit is the complement of the m^{th} bit, we note that most terms in Eqn (2 8) give a net contribution of zero The only exception are for $j = \pm 1$, with $n = m+1$ for which

$$P\left[X(m+1)=0\ 5 \mid_{X(m)=0\ 5}\right] = P\left[X(m+1)=-0\ 5 \mid_{X(m)=-0\ 5}\right] = 0, \tag{2 9}$$

and

$$P\left[X(m+1)=-0\ 5 \mid_{X(m)=0\ 5}\right] = P\left[X(m+1)=0\ 5 \mid_{X(m)=-0\ 5}\right] = 1 \tag{2 10}$$

Thus giving $R_{yy}(1) = R_{yy}(-1) = \left[-1/4(m+1)\right]$, (2 11)

and $R_{yy}(j) = 0 \ , \ |j| > 1$ (2 12)

Using the Dirac delta function notation to write the autocorrelation function for the underlying impulse process gives

$$R_{yy}(\tau) = (1/4)\left[\delta(\tau) - \left[\delta(\tau \pm 1)/(m+1)\right]\right] \tag{2 13}$$

By taking the Fourier transform of the autocorrelation funotion, we get power spectral density, which takes the form

$$S_{yy}(f) = (1/4)\left[1 - \left[2\cos(2\pi f)/(m+1)\right]\right] \tag{2 14}$$

The continuous power spectra is plotted for various values of m and is shown in Fig 2 2

2 5 2 ERROR MONITORING

When an EX-OR function is applied to two successive bits of the mB1C code, at least a mark is obtained for every m+1 bits, since the $(m+1)^{th}$ bit is the complement of the m^{th} bit However, this fails when an error occurs Such violations are used for error monitoring If continuous two bit errors are ignored, the error detection probability P_c of the C bit check can be given by $P_c = 2P_e/(m+1)$, where P_e is the bit error rate in the line

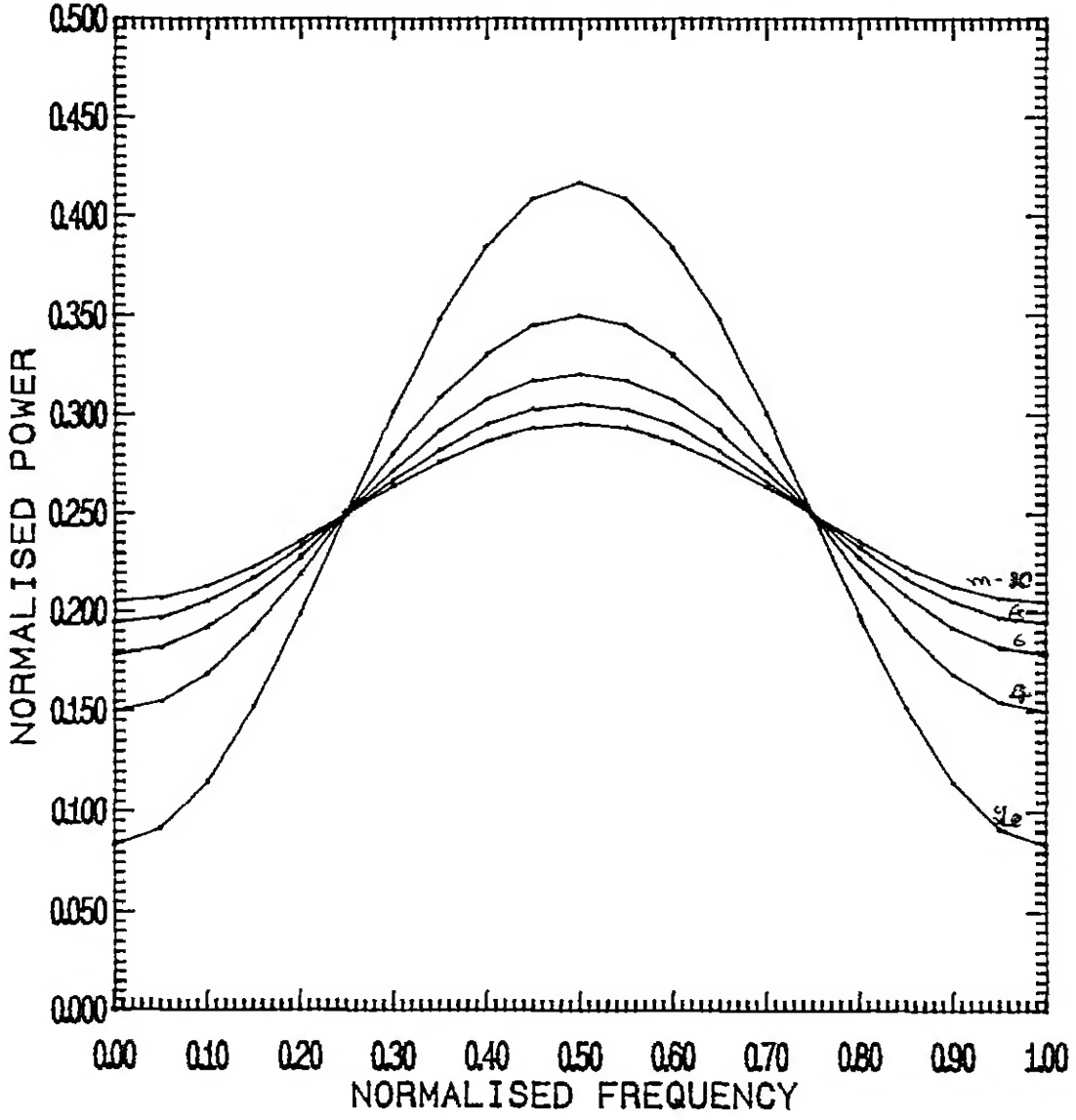


Fig 2 2 Continuous power spectra for mB1C codes

CHAPTER 3

CODER

3 1 INTRODUCTION

In this chapter, a basic block diagram representation of an mB1C coder circuit along with the timing diagram are given The timing constraints in the circuit are given in terms of the propagation delays of the integrated circuits used The circuits are then discussed in detail The PLL which is used to synchronize the two clocks in the coder circuit is also discussed

3 2 BLOCK DIAGRAM OF THE CODER

Figure 3 1 shows the block diagram of an mB1C coder The data to be coded (D_{in}), which is in a serial form is converted into parallel form by means of a serial-to-parallel converter (C1) This operation is clocked at the coder clock rate f_{cc} After every m clock cycles, a new m bit sequence has to be coded These m bits are to be latched after every m coder clock cycles To latch these m bits, two control signals DLC1 (Data Latch 1) and CP2 (Clock Pulse 2) are generated The C bit is generated by complementing the m^{th} bit These two functions are performed by the latch and complement bit inserter block (C2) Then, the m+1 bits now available in parallel form must be converted into serial output This conversion is done by first latching the m+1 bits into a parallel-to-serial

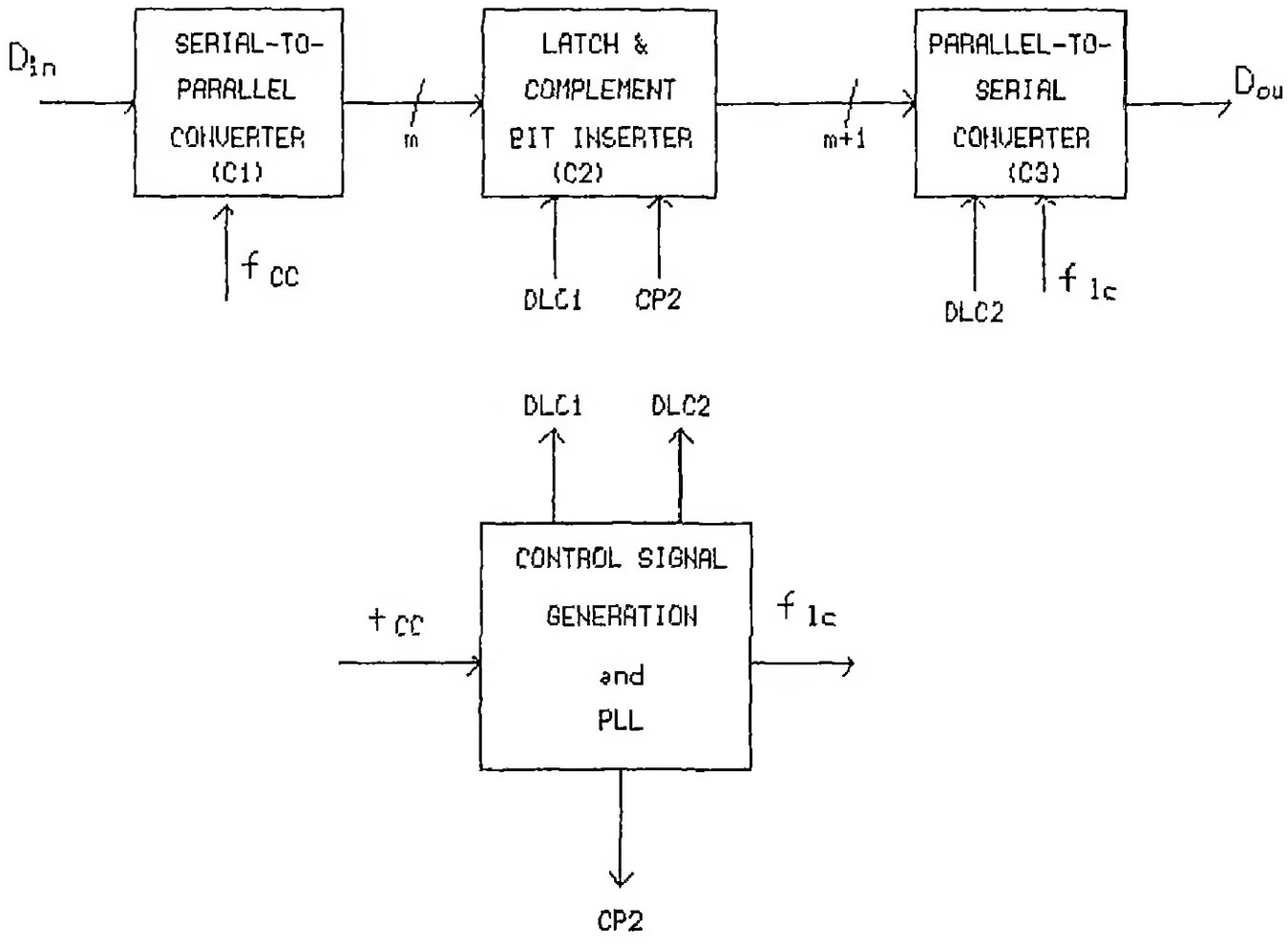


Fig 3 1 The block diagram of the mB1C coder

converter (C3) and then serially clocking them out The latching is done by the latching signal DLC2 (Data Latch 2) in the coder The clocking out is done by the line clock in the coder f_{lc} The control signals DLC1, DLC2, CP2, and the line clock f_{lc} are generated from the coder clock f_{cc} by the control signal generator and PLL block as shown in Fig 3 1

3 3 THE TIMING DIAGRAM

Figure 3 2 gives the timing diagram of the coder circuit The 4B1C code is realised in this work Coder clock f_{cc} is used to clock the incoming data, which is separated into four bit blocks and then coded DLC1 goes low once in every four coder clock pulses, hence, it actually is a divided-by-four signal CP2 is generated from the negative coder clock transition while DLC1 is low, as shown in the timing diagram DLC1 should go low before the CP2 pulse occurs, when the four data bits will be latched into the latch and complement bit inserter from the serial-to-parallel converter This is indicated in the timing diagram by Q_3 of C1 (Q_3 and Q_0 are the most significant bit and the least significant bit of C1 respectively) The high to low transition of DLC1 acts as the data trigger point Immediately after this point, the first of the m data bits should be available at the data input point of the serial-to-parallel converter This can be used by any external circuit supplying serial data to the line coder The control signal generator generates a signal PL4, which is also a divided-by-four

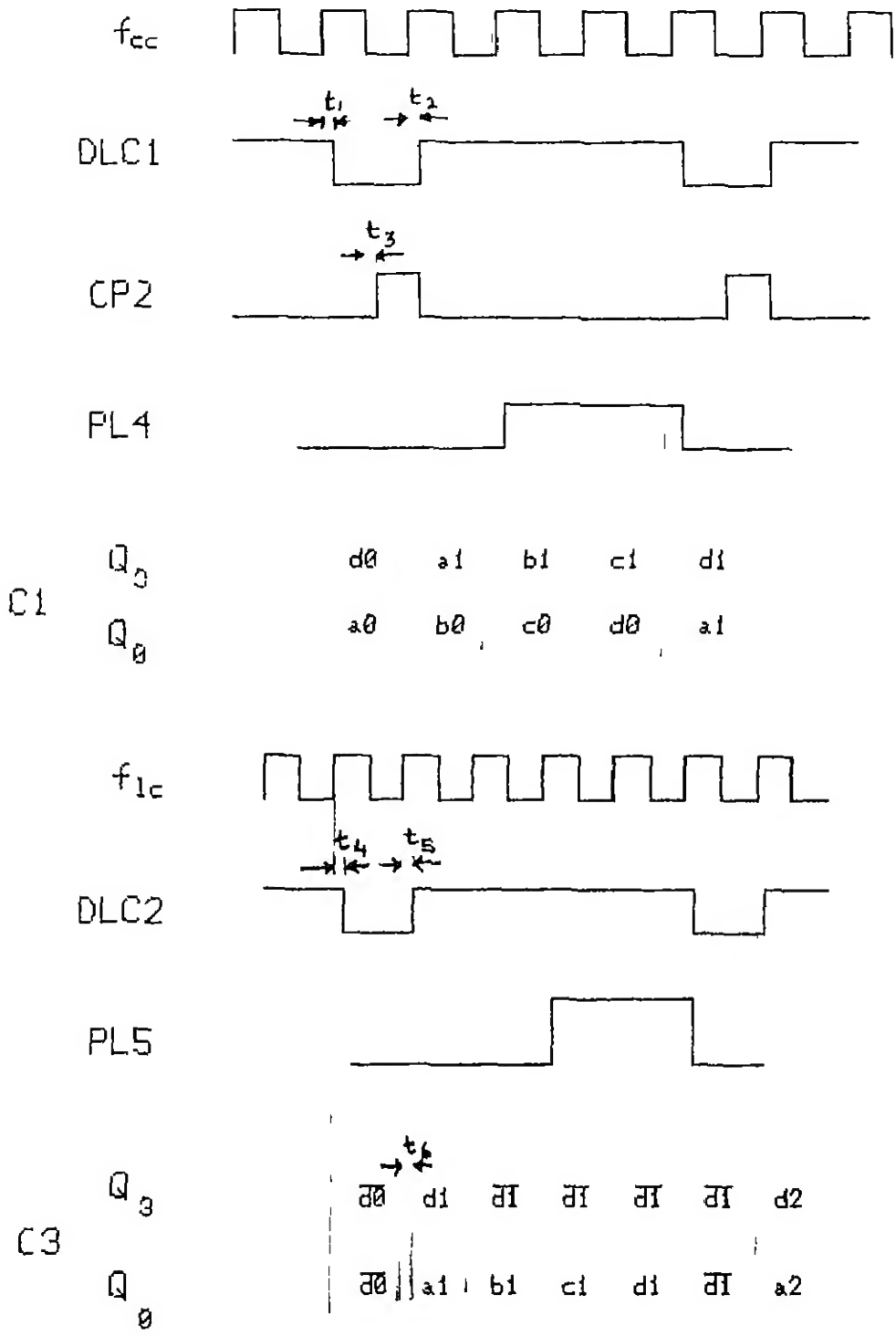


Fig 3 2 The timing diagram of the 481C coder

signal and is used by the PLL for synthesizing the line clock f_{lc}

The data is clocked out at the frequency of the line clock f_{lc}. Once in every five (m+1 = 5 for 4B1C code) line clock pulses, the data should be latched from the latch and complement bit inserter into the parallel-to-serial converter. DLC2 in coder goes low once in every five line clock periods.

When positive transition of the line clock f_{lc} occurs with DLC2 low, a new data block alongwith the complement bit is latched onto the parallel-to-serial converter. This is indicated in the timing diagram by Q_3 of C3 (Q_3 and Q_0 are the most significant bit the least significant bit of C3 respectively, and Q_0 acts as the node to serially output the data Dout). For the next four line clock pulses, the latched data gets serially out from Q_0. The timing diagram also shows the divided-by-five signal PL5 which is used by the PLL for synchronizing with PL4.

3.3.1 THE TIMING CONSTRAINTS

The important timings indicated in the timing diagram of Fig 3.2 are

t_1 - time at which DLC1 goes low, measured from the immediately preceding coder clock (f_{cc}) positive transition,

t_2 - time at which DLC1 goes from low to high, measured from the immediately preceding coder clock (f_{cc}) positive transition,

t_3 - time when CP2 goes high, measured from the immediately

preceding negative transition of coder clock (f_{cc}),

t_4 - time at which DLC2 goes from high to low, measured from the immediately preceding positive transition of the line clock (f_{lc}),

t_5 - time at which DLC2 goes from low to high, measured from the immediately preceding line clock (f_{lc}) positive transition,

t_6 - Availability of the first data in a block at Dout, measured from the immediately preceeding positive line clock transition,

$t_{cc} = 1/f_{cc}$ = coder clock period, and

$t_{lc} = 1/f_{lc}$ = line clock period

The timing constraints in the circuit are

1 $t_1 < (t_{cc}/2 + t_3)$

The signal DLC1 should go low before the positive transition of CP2, so that the correct data latching occurs from the serial-to-parallel converter to the latch and complement bit inserter For the same reason, the following condition is also given

2 $t_3 < t_{cc}/2$

3 $t_4 < t_{lc}/2$

For data to be effectively latched from the latch and complement bit inserter into the parallel-to-serial converter

4 $t_5 < t_{lc}/2$

To enable serial shifting operation in the parallel-to-serial converter

3 4 THE CIRCUIT DESCRIPTION

Our aim is to realize the coder circuit capable of working at the maximum frequency realizable with the available hardware The fastest digital integrated logic circuits available with us are the ECL (Emitter-Coupled Logic) ICs In this work, 10K and 100K series of ECL ICs are used in the coder circuit

3 4 1 THE ECL IC

The basis of all ECL circuits is the nonsaturating current switch, which is an emitter-coupled pair The high operating speed is obtained since the transistors in ECL circuits operate in the nonsaturating mode That is, the transistors do not switch fully on or fully off, but swing above and below a given bias voltage Delay time ranges from subnanosecond to tens of ns ECL generates a minimum of noise and has a considerable noise immunity However, it dissipates more power than other logic gates

With ECL gates, it is a common practice to ground the positive end of the supply voltage One advantage of using this arrangement is that it minimizes external noise transfer Therefore, a neagtive supply voltage is required, and the standard value used is -5 2 V Logic high (1) and logic low (0) for ECL circuits are at about -0 9V and -1 7V respectively, which yields a nominal voltage swing of about 0 8V

In ECL circuits, large voltage transients appear at the collector node of the output driving transistors However, the current supplied for the reference and the bias circuits should not get affected by these transients Therfore, two separate ground connections - dirty ground and clean ground are provided in the ECL 10K/100K gates The most popular form of ECL gates is the 10K series which is produced by many manufacturers [18,19]

Some highlights or general requirements in using ECL ICs are

1 ECL ciruits are nonsatuiating and so have high current requirements, and therefore, power supplies should be capable of supplying current well over 1 Amp

2 Since the voltage swing between the ECL high and low levels is only about 800 mV, it is important that the power supplies be extremely clean and free of spikes, hum, or other types of noise

3 All inputs must be terminated through a 50 Ω resistance to ground

4 To avoid oscillations, care should be taken to decouple the two grounds and the supply voltage

3 4 2 THE INTEGRATED CIRCUITS USED

The data path has a serial-to-parallel converter, a latch and a parallel-to-serial converter The chip 100136 is used for all these three purposes It operates as a four bit up/down counter or

as a four bit left/right shift register Table 3 1 gives the pin description of the chip The operating mode is fixed by the three selection inputs So, S1, and S2 as given in Table 3 2

These selection inputs also enable parallel loading, synchronous reseting, and complementing of flip-flop outputs Do and D3 are the serial inputs for left shifting and right shifting respectively A carry output $\overline{TC}$ goes low for a data of $1111_{(2)}$ (= 15_D) value in the up-counting mode, and for $0000_{(2)}$ (= 0_D) in the down-counting mode In shifting mode, it repeats the output Q3 A high level on MR enables asynchronouse master reset Two count enables, $\overline{CEP}$ and $\overline{CET}$, allow multistage counter cascading The typical propagation delay of this chip is approximately 1 8 ns

The chip 100114 is a quint (five) line receiver It has two inputs and two outputs, both direct and complement An internal reference bias is available, which when connected to one of the inputs of a gate, makes the other input to operate as a standard 100K ECL input The direct output of a gate goes low and the complementary one goes high, when both inputs are either open or have equal voltages applied on them This is used where ever a permanent low/high is required in the circuit The typical propagation delay of this chip is approximately 1 4 ns

Table 3 1

Pin description of the chip 100136

Pins	Descriptions
D_3	Serial data input
P_0 P_3	Preset Input
CP	Clock input
D_0 - $\overline{CET}$	Serial data input/Count enable trickle input
$\overline{CEP}$	Count enable parallel input
S_0 - S_2	Select input
MR	Master reset input
$\overline{TC}$	Terminal count output
Q_0 Q_3	Data outputs

Table 3 2

Selection table of the chip 100136

S_0	S_1	S_2	Operating modes (synchronous)
L	L	L	Parallel load data available on P_n will be loaded with next clock pulse
L	L	H	Down counter each clock pulse decreases the counter value
L	H	L	Right shift each clock pulse shifts D_3 to Q_3, Q_n to Q_{n-1}
L	H	H	Up counter each clock pulse increases the counter value
H	L	L	Complement mode contents of the flip-flops can be synchronously inverted
H	L	H	Reset enables a synchronous reset
H	H	L	Left shift each clock pulse shifts Q_n to Q_{n+1}, D_0 to Q_0
H	H	H	Hold mode no change for Q_n

The chip 100102 is a quint two-input OR/NOR gate with a common enable It has a typical propagation delay of approximately 0 75 ns The chip 100107 is a quint two-input Ex-OR/Ex-NOR gate with a compare output This has a typical propagation delay of

approximately 0 95 ns These gates are used in control signal generation

The chip 10136/10137 is a high speed synchronous hexadecimal/decade counter that can count up, count down, or preset The operating mode is programmed by three control lines S_0, S_1, and the clock C_P The function select table is given in Table 3 3

In the preset mode (loading step), a clock pulse is needed for the information present on the data inputs to be entered into the counter The counter changes state only on the positive going edge of the clock, therefore at other times, any input may change without affecting the status on the counter The typical propagation delay of this chip is approximately 3 3 ns One of

Table 3 3

Function select table of the chips 10136 and 10137

S_0	S_1	Operating mode
L	L	Preset (Program)
L	H	Increment (Count Up)
H	L	Decrement (Count Down)
H	H	Hold (Stop Count)

these chips can be used for divided-by-four and divided-by-five operations The chip 100136 would be a better choice for the purpose as it is faster than the chips 10136/10137 However, in our

circuits, we have used the chips 10136/10137 due to non availability of enough number of 100136 ICs

The chip 10131 is a dual master slave flip-flop It has a common clock enable independent of the two separate clocks for each of the two D flip-flops Thus, each flip-flop can be clocked separately by holding the common clock enable input low This has a typical propagation delay of approximately 3 ns They are used as D flip-flops in the circuit

MC12040 is a phase-frequency detector intended for use in systems requiring zero phase and frequency difference at lock This is a digital phase-frequency detector for use as a phase comparator for ECL compatible input signals It determines the lead or lag phase relationship and the time difference between the leading edges of the waveforms This phase detector has a range of $\pm 2\pi$ radians, and a gain of approximately 0 16 V/radian

MC1658 is a voltage-controlled multivibrator which provides appropriate level shifting to produce an output compatible with the ECL logic levels The frequency control of this chip is accomplished through the use of a single external capacitance A filter is used to help eliminate ripple on the output voltage levels at high frequencies, and the input filter is used to decouple noise from the analog input signal The 741 opamps are used for realizing the active filters

3 4 3 THE CODER CIRCUIT

The schematic of the coder circuit is shown in three parts in Figs 3 3, 3 4, and 3 5 Figure 3 3 shows the data path comprising of a serial-to-parallel converter (C1), a latch (C2) and a parallel-to-serial converter (C3) All the three stages are realized using 100136 chips by choosing proper select inputs C2 is made to latch on to the data from C1 once in every four coder clock pulses The DLC1 control signal generated by the divide-by-four circuit (C4) goes low once in every four coder clock pulses This makes S_0, S_1, and S_2 of C2 go low Data is latched from C1 to C2 when a clock is applied while DLC1 is low C3 is used as a parallel-to-serial converter by making its control signals S_0 and S_2 low S_1 has a control signal DLC2 on it which helps in latching data once in every five line clock pulses While latching, it adds the complement bit alongwith the four data bits into C3 $\overline{Q}_3$ of C2 will have the complement bit, and it is transmitted to the serial data-in D_3 of C3, while latching For other four line clock pulses, it shifts the latched data serially out DLC2 is generated by C5

The divided-by-four function which provides the control signal DLC1 is realized using the chip 10136/10137 This chip is used as an up-counter by making S_0 low Q_2 is connected to S_1 and is named as DLC1 The count is started by parallel loading a data $0101_{(2)}$ This data will enable parallel latching to occur once in every four clock pulses This makes DLC1, Q_2, and therefore, S_1

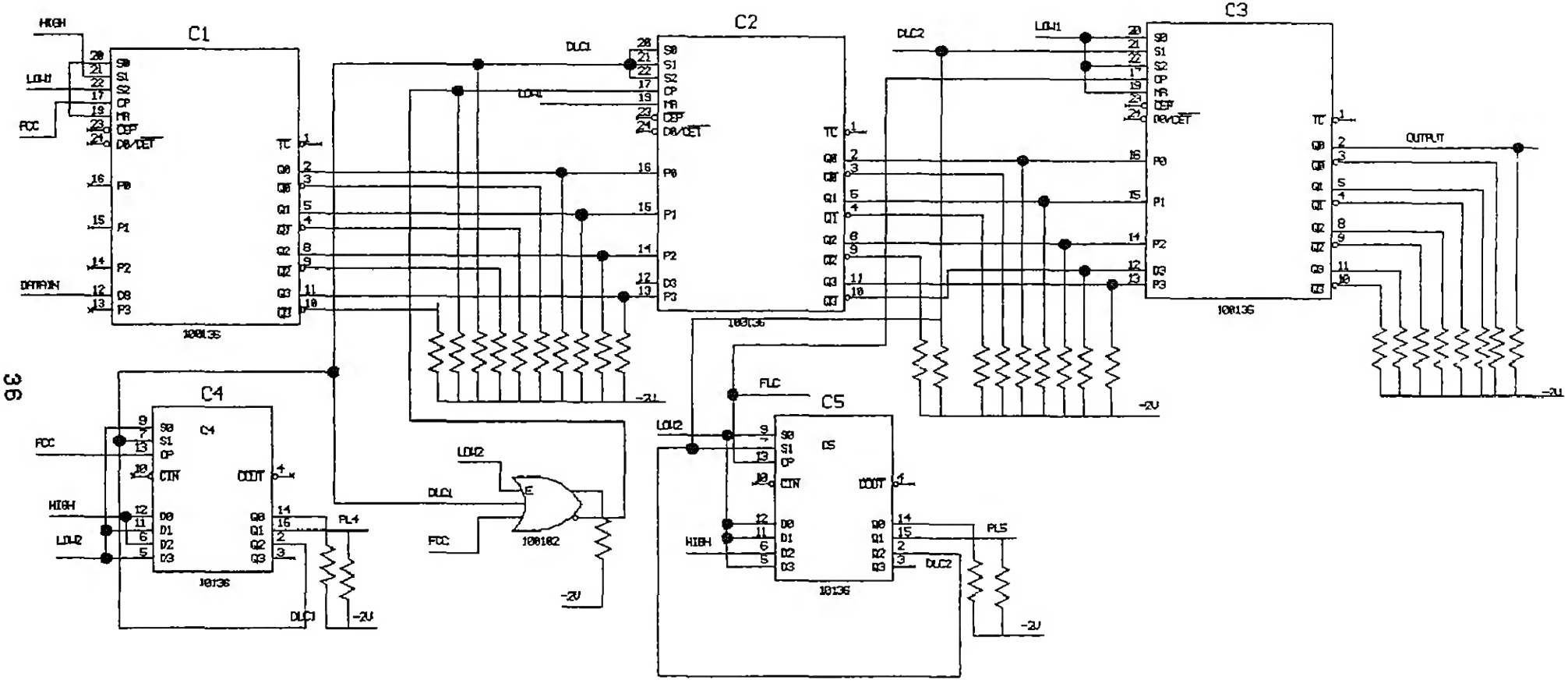


FIG 3 3 The coder circuit - part A

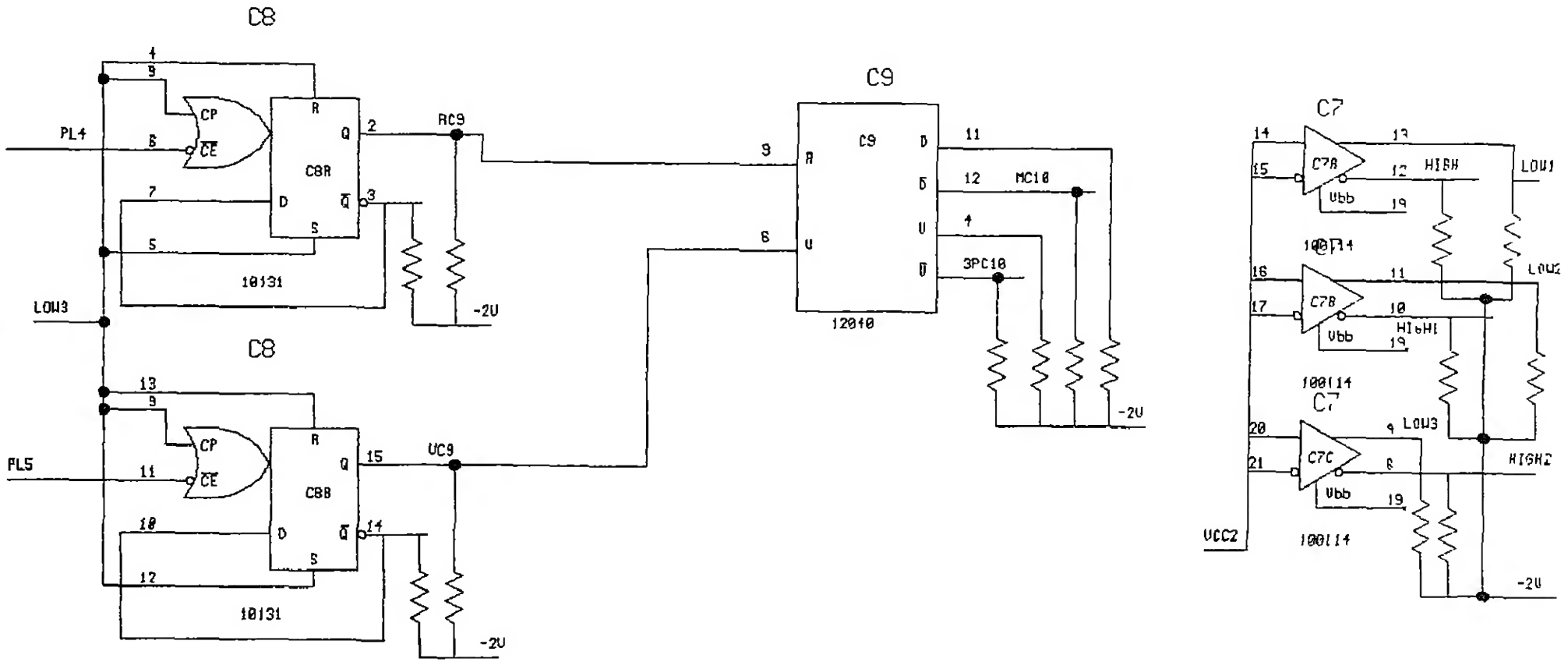


FIG 3 4 The coder circuit - part B

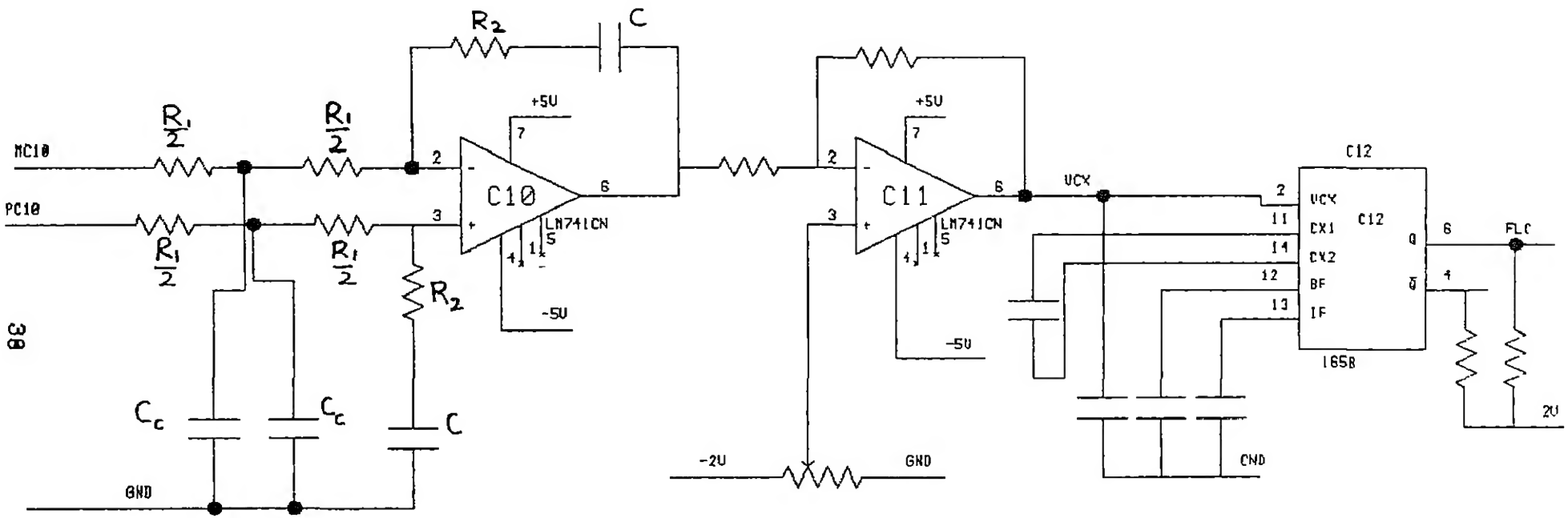


FIG 3 5 The coder circuit - part C

high, and the chip is in count-up mode After three clock pulses, the data will become $1000_{(2)}$ In the next clock pulse, DLC1 goes low and again parallel loading of $0101_{(2)}$ data occurs The divide-by-five function is realized by C5 in a similar manner, with the only difference that here the parallel data latched in is $0100_{(2)}$ This data will enable parallel latching to occur once in every five line clock pulses

The signal PL5 (= $f_{lc}/5$) in the coder should be synchronized with the signal PL4 (= $f_{cc}/4$) for the correct operation of the coder circuit As the signal PL5 does not have a 50% duty cycle, hence the signals PL4/2 and PL5/2 are used for synchronization by the PLL The 10131 chip is used as a divided-by-two (toggle) flip-flop for both the PL4 and PL5 signals The above circuit is shown by chip C8 in Fig 3 4 The chip 10131 has two D-flip-flops A D-flip-flop is converted into a T-flip-flop by connecting its complement output $\overline{Q}$ to its D input The chip C7 in Fig 3 4 is a line receiver used to generate logic low and high signals to be used in other ICs where ones and zeros are required The chip C9 in Fig 3 4 is the phase-frequency detector and the chip C10 in Fig 3 5 is the active low-pass filter used in the PLL Figure 3 5 also shows the chips C11 and C12, where C11 is used to level shift the control voltage detected by the filter, and C12 is the voltage-controlled-multivibrator The PLL is described in more detail in the following section

3 5 THE PHASE LOCKED LOOP (PLL)

A phase locked loop (PLL) basically consists of a phase detector, a loop filter, and a voltage-controlled oscillator [8,9], as shown in Fig 3 6 The basic [illegible] theory of the PLL is given in appendix A Among other applications, it can be used as a frequency synthesizer or as a narrow-band filter, tracking the input frequency

Good tracking performance requires large gain The loop which normally is in its quiescent state, must be brought into the lock mode This operation is called the acquisition The time required to lock is called the acquisition time It is possible to bring the loop into self lock, only if the input frequency is within the capture or the pull-in range of the loop The PLL remains in the locked state so long as the input frequency is within its lock range

3.5.1 THE PLL FREQUENCY SYNTHESIZER

In the coder circuit discussed, the line clock f_{lc} has to be synthesized from the coder clock f_{cc}, such that f_{cc}/m is equal to $f_{lc}/(m+1)$ The PLL can be used as a frequency synthesizer, which can produce a precise frequency derived from another stable source A basic block diagram of a PLL frequency synthesizer is shown in Fig 3 7

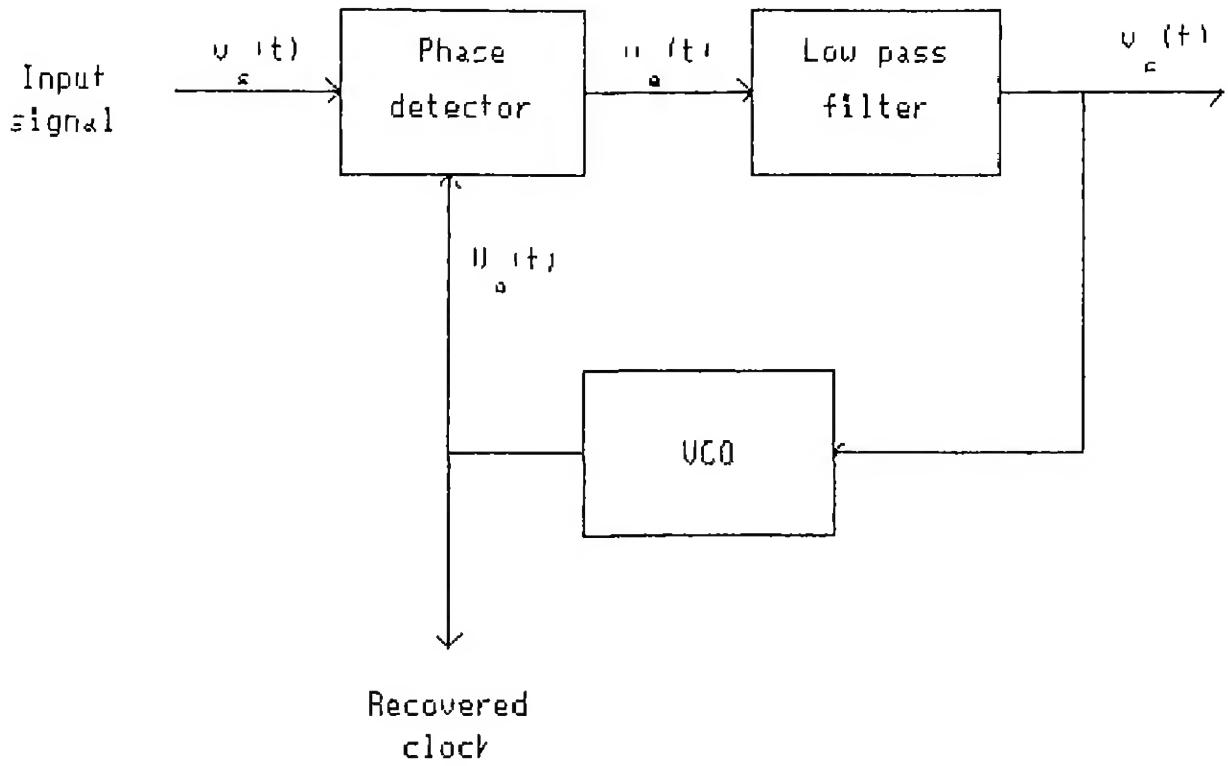


Fig.3.6 The block diagram of a PLL.

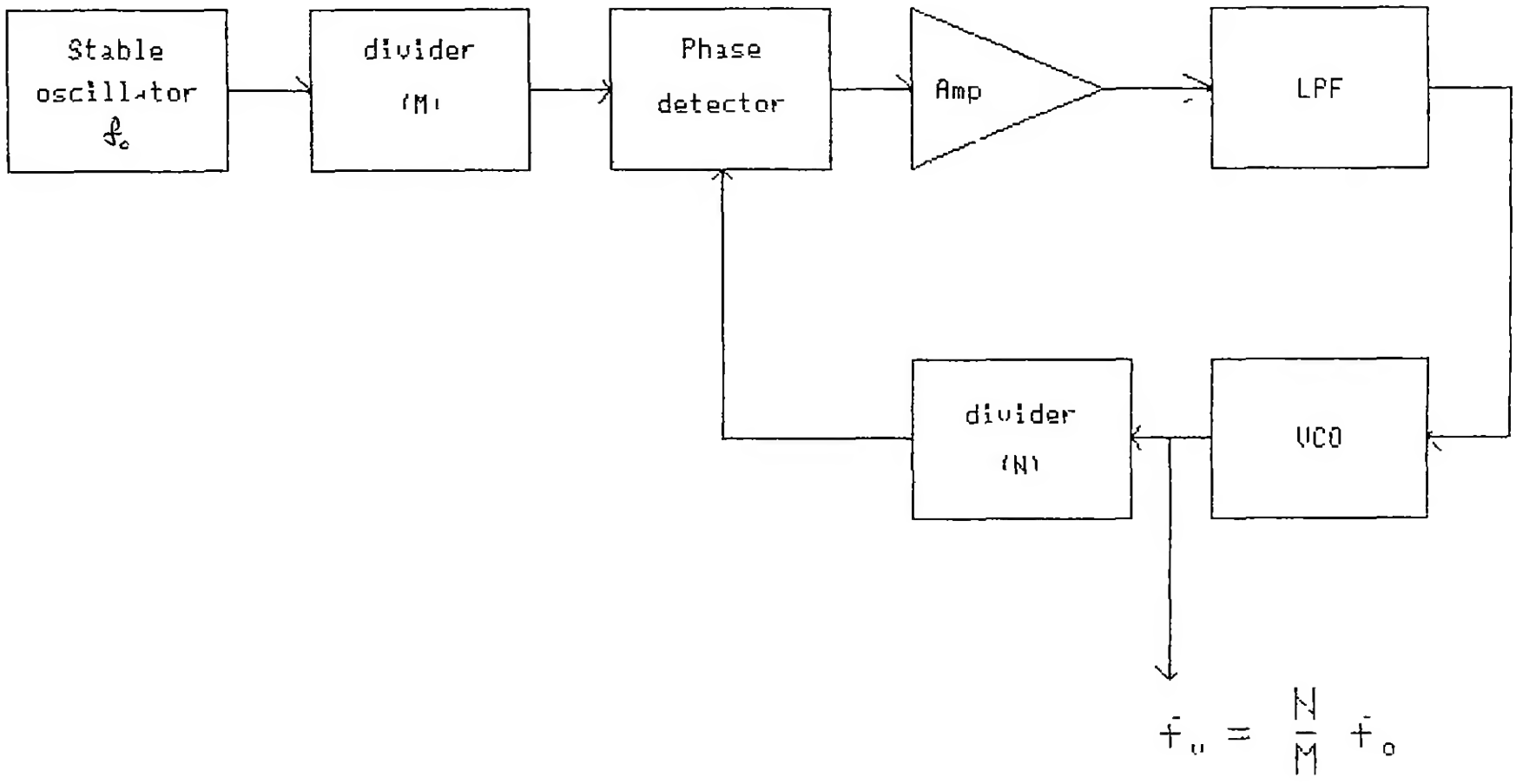


Fig. 3.7 A PLL used as a frequency synthesizer

The synthesizer consists of a source at a frequency f_o and a VCO at a frequency f_v The source frequency f_o is divided by an integer M and the VCO frequency is divided by another integer N The two resultant waveforms are than compared by a phase detector Phase locking imposes the condition that f_o/M must equal to f_v/N, so that the output frequency f_v is locked to a rational fraction of the stable oscillator frequency f_o The long term stability and accuracy of the output frequency therefore are the same as that of the reference multiplied by N/M The short term stability, on the other hand, is that of the reference times N/M if the loop bandwidth is large, and is that of the VCO if the loop bandwidth is small

The phase locked synthesizer offers a means of generating the line clock f_{lc} from the coder clock f_{cc} This can be achieved with M = m and N = m+1 In this case, of course, f_{cc} is equal to f_o and f_{lc} is equal to f_v When N or M is an odd term, the output of the divider is a non-50% duty cycle pulse To make both f_{lc}/N and f_{cc}/M as 50% duty cycle signals, N and M are made equal to 2(m+1) and 2m respectively in the implementation of the coder circuit This division also provides another advantage of overcoming the frequency limitation of the phase-frequency detector

3.5.2 THE DESIGN AND IMPLEMENTATION

The PLL frequency synthesizer realized makes use of the chip MC1658 as the voltage-controlled multivibrator (VCM) The

center frequency of the VCM can be fixed by selecting the external timing capacitor Figure 3 8, which shows the frequency-capacitance product as a function of the control voltage, helps in the selection of the timing capacitor [19] The gain constant of the VCM is measured experimentally Table 3 4 gives the variation of the VCM center frequency f_o and the gain constant K_v with the control voltage V_c It is observed that K_v is approximately equal to 314 Mrad/sec/V The phase detector used is MC12040 and it has a gain constant K_d of 0 16 V/rad

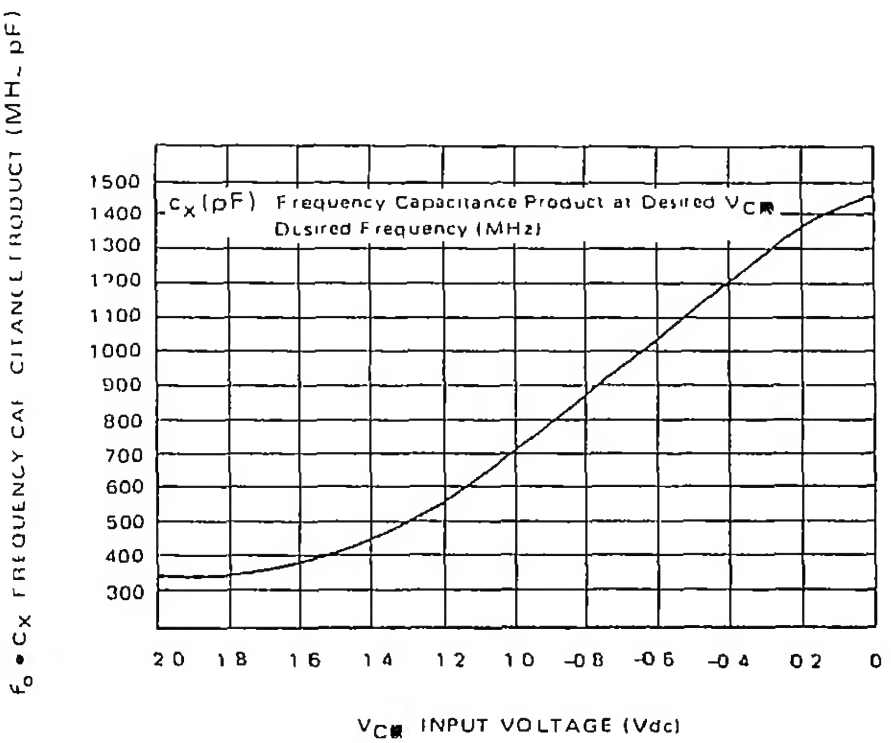
Table 3 4

Variation of the VCM frequency f_o and the gain constant K_v with respect to the control voltage V_c

V_c (mV)	f_o (MHz)	K_v Mrad/sec/V
- 500	100	
- 750	79	
-1000	65	351
-1250	52	326
-1500	40	301
-1750	34	

The loop filter is the single most important part of any PLL To minimize the output phase jitter due to noise, the loop bandwidth should be as narrow as possible [8,9] On the other hand,

Fig 3 8 The frequency-capacitance product versus the control voltage V_c for the VCM MC1658



for best tracking and acquisition properties, the loop bandwidth should be made as wide as possible [8,9] Hence, clearly there is a trade-off involved The capture time depends on the amount of the loop gain and the bandwidth of the loop filter Reducing the loop bandwidth has the following consequences

1 improved rejection of out-of-band signals,

2 decrease in the capture range, and

3 longer acquisition time

For the frequency synthesizer designed in this work, an active filter with a low loop bandwidth is used The frequency of the coder clock should be stable for the line clock to be stable C10 in the Fig 3 5 shows the schematic of the active filter used

The following design specifications are used for the PLL employed in the coder circuit Please refer to Appendix A for more details

1 The phase detector gain is

$$K_d = 0\ 16\ V/rad$$

2 The VCO gain is

$$K_v = 3\ 14 \times 10^8\ rad/sec/V$$

3 $N = 2(m+1) = 10$ (for 4B1C coding)

4 The loop gain is

$$K = (K_d K_v/N)\ rad/sec,$$

$$= 5 \times 10^6\ rad/sec$$

The unit of the phase detector gain is given by V/rad when

the linear model is considered with a very small phase error, such that $\sin\theta \cong \theta$ Otherwise, it acts as a multiplier and its the unit for the gain is given by Volts as $\sin\theta$ is a number Therefore, the unit of K is given by rad/sec

4 The damping constant δ is chosen to be equal to 0 707, i e , the system is critically damped

5 The loop bandwidth is selected to be 440 KHz

Hence,

$$\omega_n = 2\ 76 \times 10^{6} \text{ rad/sec}$$

Now,

$$\tau_1 = R_1C = K/(\omega_n)^2 = 656 \times 10^{-9} \text{ sec},$$

$$\frac{\tau_2}{\tau_1} = \frac{R_2}{R_1} = \frac{2\delta\omega_n}{K} = 0\ 7805$$

The high frequency spikes appearing at the output of the phase detector have to be snubbed such that they do not affect the performance of the filter This is achieved by splitting R_1 and adding a snubber capacitor C_c (please refer to Fig 3 5) The value of C_c is selected such that the time constant $(R_1/2)C_c$ is less than that of R_2C

From the above relations we get

$R_1/2 = 3\ 3\ k\Omega$,

$R_2 = 5\ 6\ k\Omega$,

$C = 100\ pF$, and

$C_c = 3\ 3\ pF$

Some of the important parameters of the PLL are calculated below

1 Lock range

$$f_l = \pm KN/2\pi \text{ MHz},$$
$$= \pm 8 \text{ MHz}$$

2 Velocity constant

$$K_\gamma = (K_d K_v \tau_2)/\tau_1,$$
$$= 39.2 \times 10^6 \text{ rad/sec}$$

3 Capture range

$$f_c = \sqrt{K_\gamma NK}/2\pi \text{ MHz},$$
$$\cong 7.05 \text{ MHz}$$

4 Noise bandwidth

$$B_l = \omega_n/2\left(\delta + \frac{1}{4\delta}\right) \text{ MHz},$$
$$= 1.46 \text{ MHz}$$

Here, the dimension of B_l is defined to be in the unit Hz, despite the fact that ω_n is given in rad/sec [8]

5 Acquisition time

$$T_p = \frac{4.2 (\Delta f)^2}{B_l^3} \text{ sec},$$
$$\cong 135 \ \mu\text{sec for } \Delta f = 10 \text{ MHz},$$

where Δf indicates the initial deviation of 10 MHz in the signal to be tracked, from the center frequency

3 6 PERFORMANCE OF THE CODER CIRCUIT

The mB1C coder circuit is made on a specifically designed PCB (printed circuit board) using the PCAD software Ground planes are added in the PCB wherever possible to reduce interference between lines

The PLL is tested and the measured parameters of the PLL are lock range = +10 MHz to -9 MHz, where + and - indicate frequencies above and below the center frequency respectively, and capture range=+9 MHz to -8 3 MHz The coder circuit is tested initially with a data stream of 1010 pattern Then it is tested with the data generated from a PRBS generator alongwith the decoder

3.7 CONCLUSION

In this chapter, the block diagram representation of a coder circuit and the timing diagram were described By performing a timing analysis it was seen that the circuit speed was limited by the switching speed of the ICs used The ICs used were of the ECL 10K and 100K series and were capable of working beyond 140 Mbps The PLL was also discussed and the calculated and the obtained values for its performance were given The capture range and the lock range obtained were found to be satisfactory The circuit works satisfactorily upto 100 Mbps however, it was observed that when the frequency was raised beyond 100 Mbps, there was a lot of interference and the signal level went down

CHAPTER 4

THE DECODER AND THE BIT SYNCHRONIZER

4.1 INTRODUCTION

In this chapter, the block diagram representation of an mB1C decoder alongwith its timing diagram, and the timing constraints of the circuit are described The bit synchronizer, the decoder circuit, and the word synchronizer are also discussed

4 2 BLOCK DIAGRAM OF THE DECODER

The block diagram of an mB1C decoder along with a bit synchronizer is given in Fig 4 1 The input line clock in the decoder (f_{ld_1}) is generated from the data received by the receiver by using a bit synchronizer' The data to be decoded arrives in a serial form, which is converted into parallel form by a serial-to-parallel converter (D1) This operation is clocked at the rate of the decoder line clock f_{ld} After every (m+1) clock cycles, we have a new (m+1) bit sequence, which has to be decoded

In mB1C code, a complement of the m^{th} bit is inserted at the $(m+1)^{th}$ bit in every block At the decoder, only the m data bits are latched and the complement bit is dumped Two control signals DLD1 (Data Latch 1 in Decoder) and D2C (Decoder clock pulse - 2) are used for this purpose by the latch block (D2)

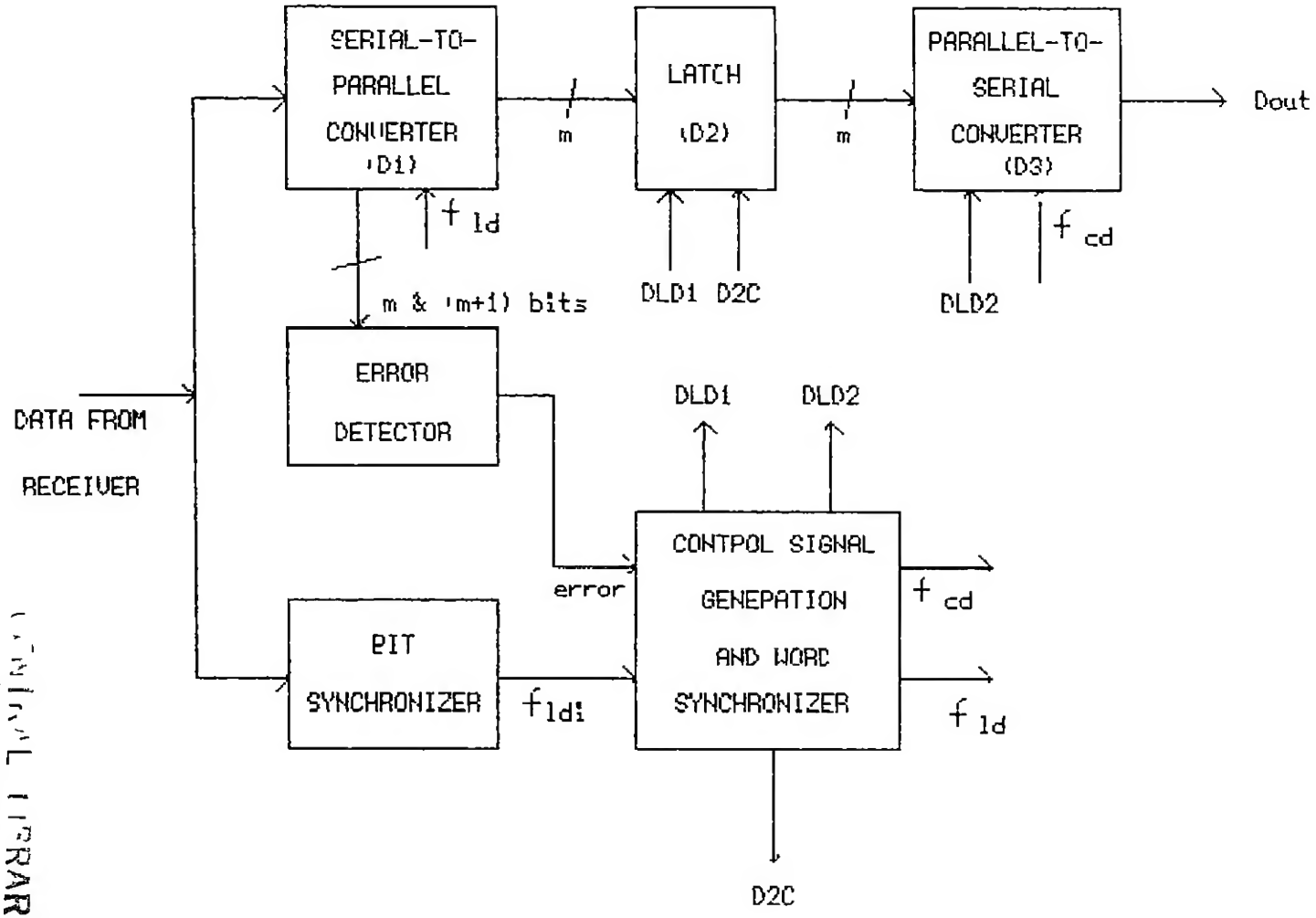


Fig 4 1 The block diagram of an mBlC decoder

The decoded data is now converted into serial output by the parallel-to-serial converter block (D3) The control signal DLD2 (Data latch 2 in decoder) is used to latch the decoded data from the latch into the parallel-to-serial converter, and then to serially clock them out The parallel-to-serial converter is clocked by the decoder clock f_{cd}

The control signals DLD1, DLD2, D2C, and the decoder clock f_{cd} are all generated in the control signal generator and word synchronizer block The frame error indicator is used to generate the error signal It checks if the m^{th} bit and the $(m+1)^{th}$ bit are complementary If it is not so, an error signal is generated which forces the word synchronizer to skip a clock pulse in the decoder line clock f_{ld}

4.3 THE TIMING DIAGRAM

Figure 4 2 gives the timing diagram of the 4B1C code decoder realized in this work In the figure, f_{ld} is the line clock in the decoder, which is obtained from the word synchronizer and is used to clock the incoming coded data In 4B1C code, the data is separated into 4 bit blocks and then coded Therefore, the incoming data should be separated into five bit coded blocks This is achieved by the DLD1 pulse indicated in the timing diagram, which goes low once in every five line clock periods in the decoder (f_{ld}), and hence, it is actually a divided-by-five signal The negative

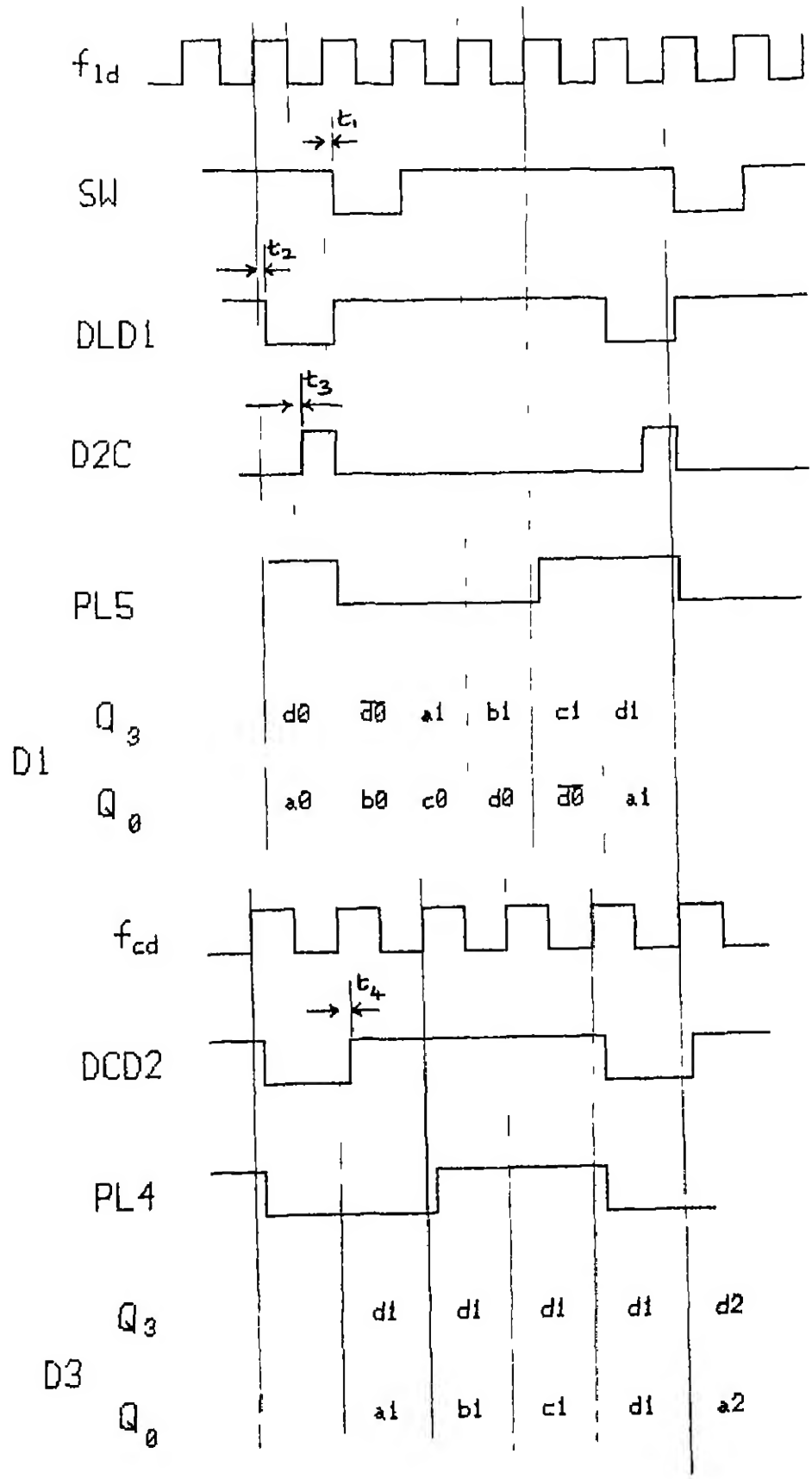


Fig.4 2 The timing diagram of the 4B1C decoder

transition of DLD1 indicates that a new data block has been decoded and is available for latching into the latch The actual latching is done by the signal D2C (decoder clock pulse - 2) signal DLD1 should go low before the D2C pulse occurs, when the decoded data will be latched into the latch Q3 and Q1 of D1 (Q3 and Q1 indicating the most significant bit and the least significant bit of the serial-to-parallel converter D1) indicate the decoded data which is going to be latched on to the latch when the pulse D2C occurs The SW (word synchronizer) indicated is also a divided-by-five signal and is used to generate the error signal When SW is low, then the m^{th} and the $(m+1)^{th}$ bits are Ex-ORed and the error signal is obtained, which is used by the word synchronizer The control signal generator generates a signal (PL5), which is also a divided-by-five signal This is used by the PLL in the control signal generator block for synthesizing the decoder clock f_{cd}

The decoded data is clocked out at the frequency of the decoder clock f_{cd} Once in every four decoder clock periods, the data is latched from the latch' on to the parallel-to-serial converter before clocking out This function is achieved by the DCD2 (data latch - 2 in decoder) pulse, which goes low for this operation DCD2 is a divided-by-four pulse, going low once in four decoder clock periods f_{cd} The positive transition in DCD2 indicates the start of a new block of data at the output This is indicated in the timing diagram by Q_9 and Q_0 of D3 (Q_9 and Q_0 indicating the most significant bit and the least significant bit of

the parallel-to-serial converter D3 respectively, of which Qo acts as the node to serially output the data Dout) The timing diagram also shows the divided-by-four signal PL4, which is used by the PLL for its synchronization with the PL5 signal

4 3.1 THE TIMING CONSTRAINTS

The important timings of the decoder circuit indicated in Fig 4 2 are

1 t_1 - time at which the word synchronizer pulse (SW) goes low, measured from the immediately preceding positive transition of the line clock in the decoder (f_{ld}),

2 t_2 - time at which DLD1 goes low, measured from the immediately preceding positive transition of f_{ld},

3 t_3 - time for D2C to go high, measured from the immediately preceding positive transition of f_{ld},

4 t_4 - time at which DCD2 goes high, measured from the immediately preceding positive transition of f_{cd}

The timing constraints in the circuit are

1 SW should go low before the next f_{ld} pulse occurs, so that the error signal can be generated, therefore

$$t_1 < t_{ld}, \text{ where } t_{ld} = 1/f_{ld}$$

2 DLD1 should go low (t_2) before D2C occurs (t_3) for correct latching of the decoded data block from the serial-to-parallel converter into the latch , therefore

$$t_2 < t_3 + \frac{t_{1d}}{2}$$

3 t_3 itself should occur before the next line clock occurs in the decoder, as the data will then change, therefore

$$t_3 < \frac{t_{1d}}{2} \text{ , and so}$$

$$t_2 < \frac{t_{1d}}{2}$$

4 DCD2 should go high before a new f_{cd} clock arrives, therefore

$$t_4 < t_{cd} \text{ , where } t_{cd} = 1/f_{cd}$$

More restrictions on timing is imposed by the word synchronizer circuit These restrictions are considered in Section 4 5

4.4 THE BIT SYNCHRONIZER

The bit synchronizer is an important subsystem of a receiver in a digital communication system Its characteristics directly influence the bit error rate, which is the usual performance measure of a digital communication system

Of the various types of bit synchronizers available [20], the nonlinear filter bit synchronizer is selected for implementation, as it is relatively simple, inexpensive and the most widely used type of synchronizers An adequate number of data transitions are essential for effective functioning of this type of bit synchronizer This is ensured by the mBIC line coding The NRZ data does not have a discrete spectral component at the bit rate The data is passed through a nonlinearity, to produce a spectral

line at the bit rate A PLL is used to extract the timing waveform The general block diagram of a bit synchronizer is given in Fig 4 3 The phase-detector, the loop filter, and the VCO form the PLL which extracts the clock signal

The efficient design of a synchronizer lies in the selection of a suitable nonlinearity and selecting the values of the parameters of the PLL to optimize the performance criterion chosen Various types of nonlinear filter synchronizer schemes available are

1 the even law nonlinearity-filter synchronizer,
2 the delay and multiply bit synchronizer,
3 the differentiate and square synchronizer, and
4 the delay and Ex-OR synchronizer

In the even law nonlinearity-filter synchronizer, the nonlinearity used is a square law device as shown in Fig 4 4(a) The implementation is simple as it makes use of diodes as the square law devices The 'delay and multiply bit synchronizer shown in Fig 4 4(b) operates on the signal by forming the product

$$m(t) = s(t)s(t-\delta),$$

where s(t) is the received rectangular random pulse signal The product waveform contains a spectral component corresponding to the bit rate 1/T, which the PLL is required to track These two types of synchronizers are attractive provided the input SNR (signal to

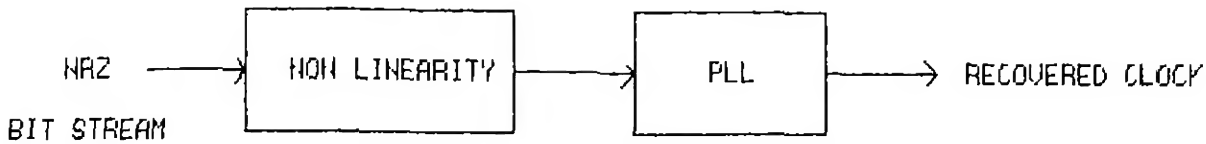


Fig 4 3 The block diagram of a bit synchronizer

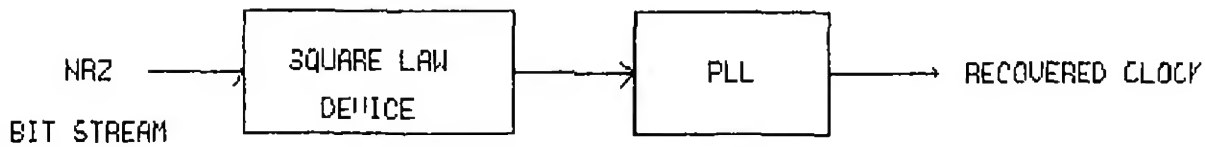


Fig 4 4(a) The even law nonlinearity type of bit synchronizer

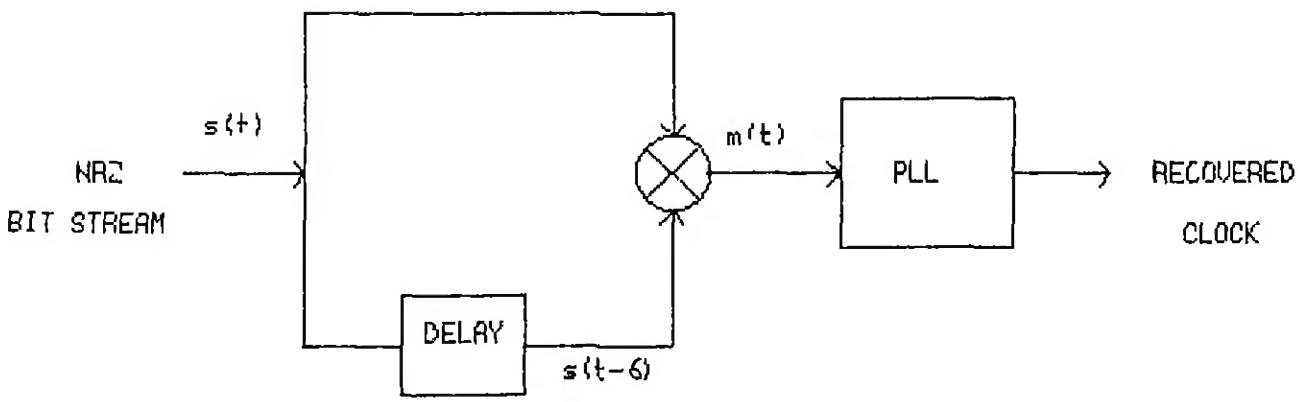


Fig 4.4(b) The delay and multiply type of bit synchronizer

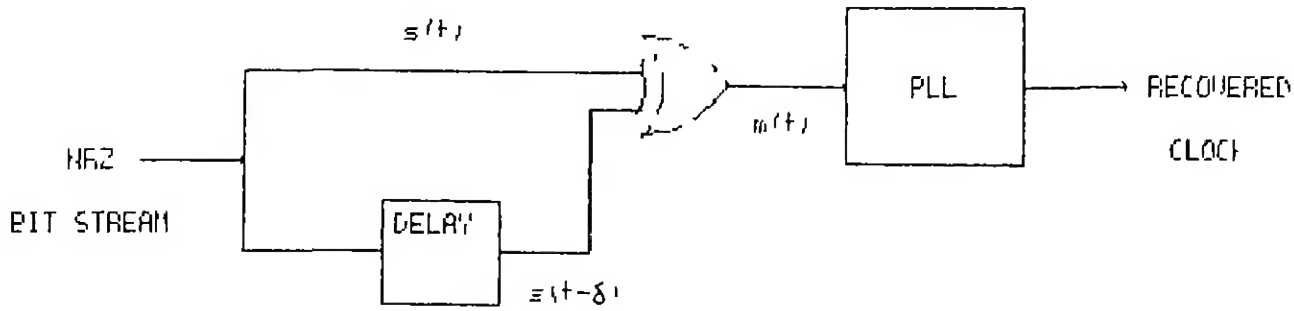
noise ratio) is large

The differentiate and square synchroniser is a transition detector The received data is differentiated, which produces positive and negative spikes for square data A full-wave rectifier converts the negative spikes into positive ones, so that at the output of the squarer, we have a positive pulse corresponding to each transition in the data, and therefore, there will be a spectral component at the bit rate

The delay and Ex-OR synchronizer was proposed by Feher [11], in which the conventional analog nonlinear processing as performed in the above three cases was replaced by digital processing The digital type of nonlinearity used is an Ex-OR gate and it also acts as a transition detector Figure 4 5 shows the circuit configuration of the delay and EX-OR synchronizer and the waveforms at different points in the circuit From practical implementation point of view, the Ex-OR gate is much easier to use and cheaper compared to the multiplier, and hence, the synchronizer developed in this work uses Ex-OR type of nonlinearity

4 4 1 DESIGN AND IMPLEMENTATION OF THE BIT SYNCHRONIZER

Figures 4 6 and 4 7 show the actual circuit diagram of the bit synchronizer used The data signal is received through a line receiver 100114 (D7) The NRZ data received is called DIN A



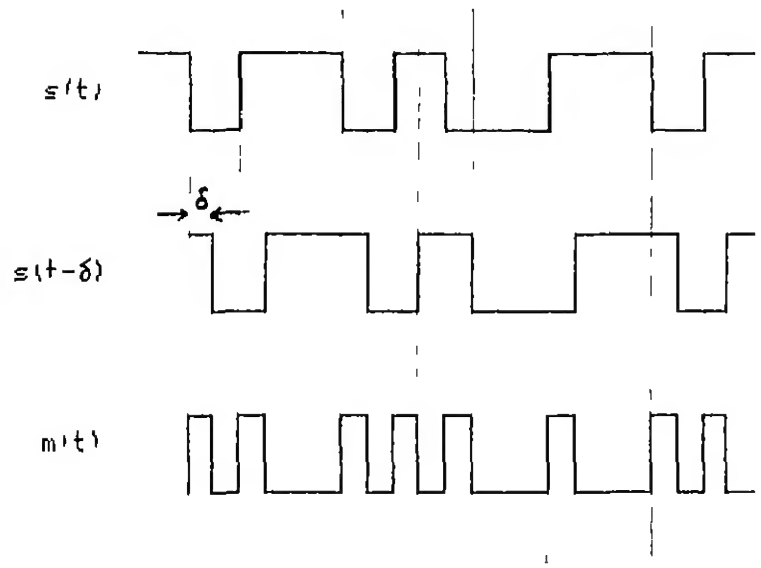


Fig 4 5 The Delay and Ex-Or type of Bit synchronizer

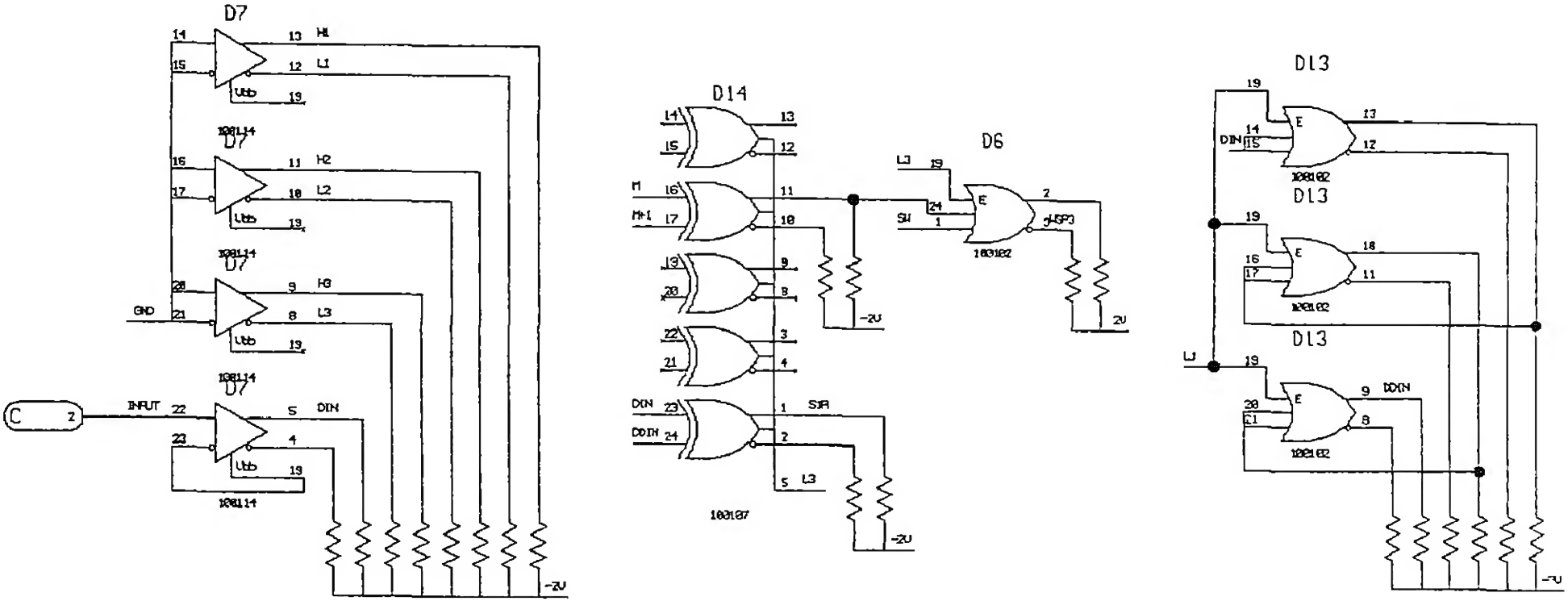


Fig 4 6 The bit synchronizer circuit - Part (a)

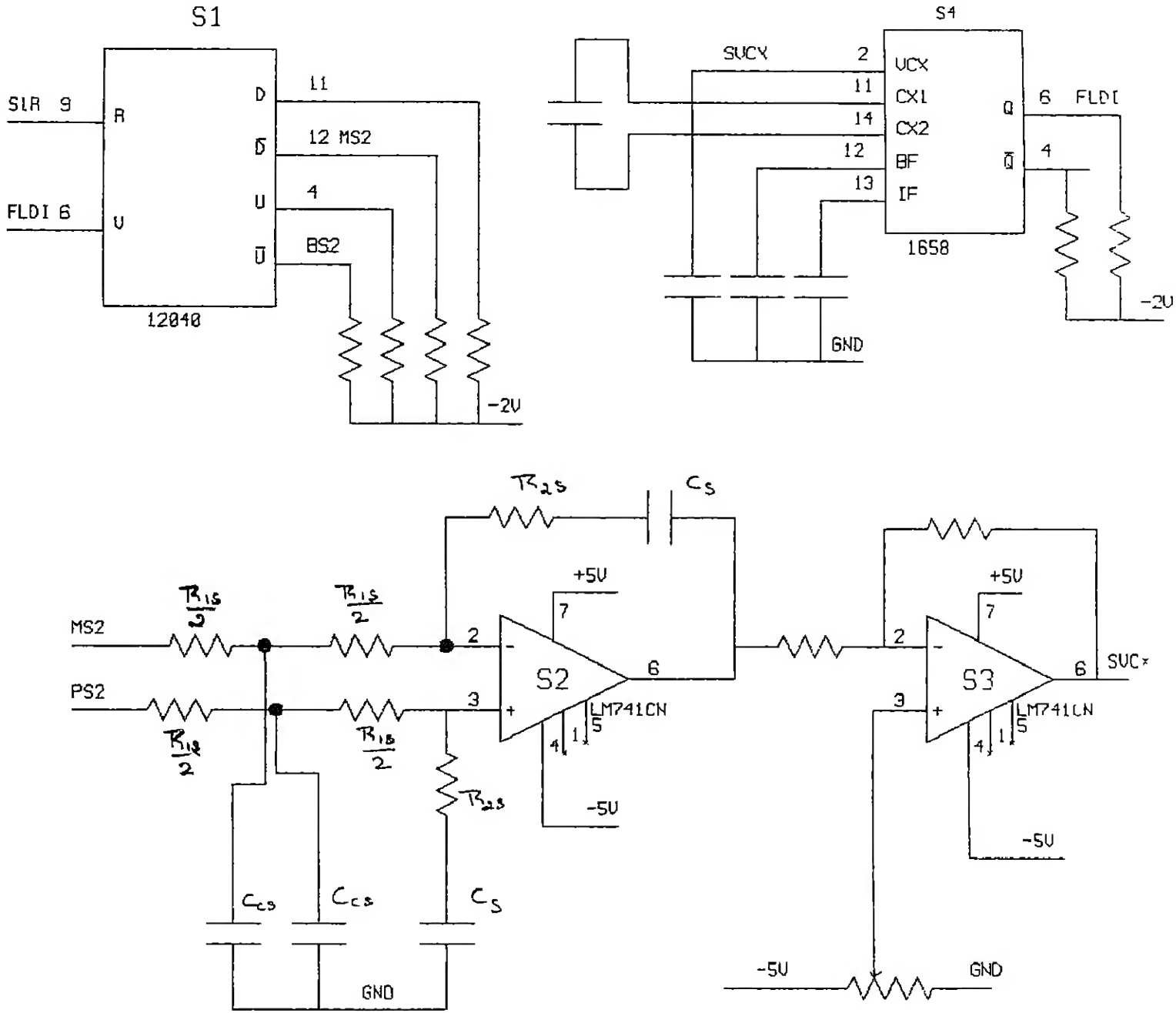


Fig 4 7 The bit synchronizer circuit - Part (b)

delayed DIN is generated by propagating the signal through three OR gates in the chip 100102 (D13) The delayed NRZ data is called DDIN The NRZ data DIN and its delayed version DDIN are Ex-ORed in an Ex-OR gate of the chip 100107 (D14) This generates a signal which is named as S1R signal it has a spectral line at the data rate and is filtered by using a PLL

The PLL is shown in Fig 4 7 It has a digital phase-detector MC12040 (S1), with a gain of 0 16 V/rad, an active low-pass filter (S2), and a voltage-controlled multivibrator (VCM) MC1658 (S4), whose center frequency can be selected by using an external timing capacitor as explained before in Chapter 3 In Fig 4 7 S3 is used to level shift the control voltage so that it lies between 0 and -2 V, which is the control voltage range of the VCM

The PLL circuit designed for the bit synchronizer is the same as the one explained in Section 3 5 2 The following design specifications are used for the PLL implemented

1 The phase-detector gain is

$$K_d = 0\ 16\ V/rad$$

2 The VCO gain is

$$K_v = 3\ 14 \times 10^8\ rad/sec/V$$

3 As we do not use any frequency divider in the feedback path of the bit synchronizer PLL, we have

$$N = 1$$

4 The loop gain is

$$K = (K_d K_v / N) \text{ rad/sec}$$

$$K = 50 \times 10^6 \text{ rad/sec}$$

4 The damping constant δ is chosen to be equal to 0 707, i e , the system is critically damped

5 The loop bandwidth is selected to be equal to 5MHz

Hence,

$$\omega_n = 31\ 42 \times 10^6 \text{ rad/sec}$$

Now,

$$\tau_1 = R_{1s} C_s = K/(\omega_n)^2 = 50 \times 10^{-9} \text{ sec},$$

$$\frac{\tau_2}{\tau_1} = \frac{R_{2s}}{R_{1s}} = \frac{2\delta\omega_n}{K} = 0\ 888$$

6 The spike suppressing capacitorC_{cs} can be found as beforeby chossing

$$10(R_{1s}/2)C_{cs} \geq R_{2S} C_s$$

From the above relations, we get

$R_{1s}/2 = 2\ 4\ k\Omega$,

$R_{2s} = 4\ 2\ k\Omega$,

$C_s = 10$ pF, and

$C_{cs} = 100$ pF

Some of the important parameters of the PLL are calculated below

1 Lock range

$$f_l = \pm KN/2\pi \text{ MHz}$$
$$= \pm 8 \text{ MHz},$$

2 Velocity constant

$$K_\gamma = (K_d K_v \tau_2)/\tau_1,$$
$$= 44\ 6 \times 10^6 \text{ rad/sec}$$

3 Capture range

$$f_c = \sqrt{K_\gamma NK}/2\pi \text{ MHz},$$
$$\cong 7\ 5 \text{ MHz}$$

4 Noise bandwidth

$$B_l = \omega_n/2\left(\delta + \frac{1}{4\delta}\right) \text{ MHz},$$
$$= 16\ 65 \text{ MHz}$$

5 Acquisition time

$$T_p = \frac{4\ 2\ (\Delta f)^2}{B_l^3} \text{ sec},$$

$$\cong 0\ 09\ \mu\text{sec for } \Delta f = 10 \text{ MHz}$$

where Δf indicates the difference in frequency to be tracked from the center frequency

The PLL bit synchronizer is tested and the important parameters are measured and are as follows

1 Lock range +10 MHz to -4 MHz

2 Capture range +8 5 MHz to -3 5 MHz

The bit synchronizer is tested initially with a data stream of 0101 pattern, then it is tested with the data generated from a PRBS generator

4 5 THE DECODER CIRCUIT DIAGRAM

The decoder circuit is shown in three parts in Figs 4 8, 4 9, and 4 10 In the decoder circuit, the ICs used are the same as those used in the coder circuit Please refer to Section 3 4 2 for the details of the ICs used Figure 4 8 shows the data path in the decoder, which consists of a serial-to-parallel converter (D1), a latch (D2), and a parallel-to-serial converter (D3) All the three stages are realized using the 100136 chips The select signals S_0 and S_2 of D1 are kept low and S_1 is made high, such that it acts as a serial-to-parallel converter D2 is made to latch to the decoded data from D1 once in every five decoder line clock periods t_{ld} The latching is done by two control signals DLD1 and D2C (decoder clock - 2), such that the $(m+1)^{th}$ bit will not be latched from D1 to D2 When DLD1 goes low, S_0, S_1, and S_2 of D2 goes low, and D2 will latch data from the serial-to-parallel converter when the D2C pulse appears The decoded data is then clocked out serially from D3 S_0 and S_2 are kept low and when DLD2 goes low, the data is latched from the latch D2 into the parallel-to-serial converter D3 On the other hand, when DLD2 goes high, the data is serially clocked out DLD2 is thus a divided-by-four pulse, going low once in every four decoder clock periods t_{cd} D6 shown in Fig 4 8 is an OR/NOR gate (100102) It is used for the generation of the control signals

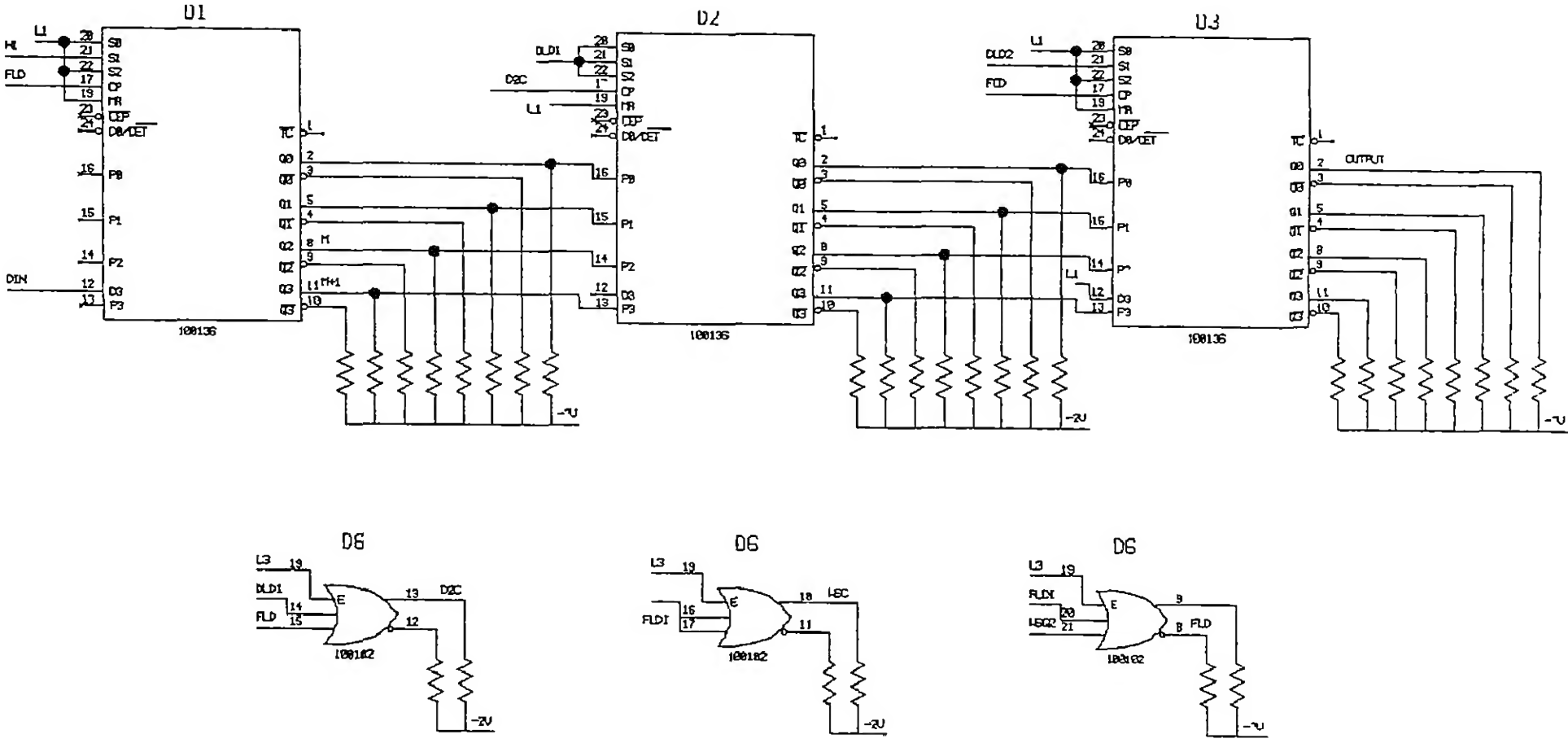


Fig 4 8 The decoder circuit - Part (a)

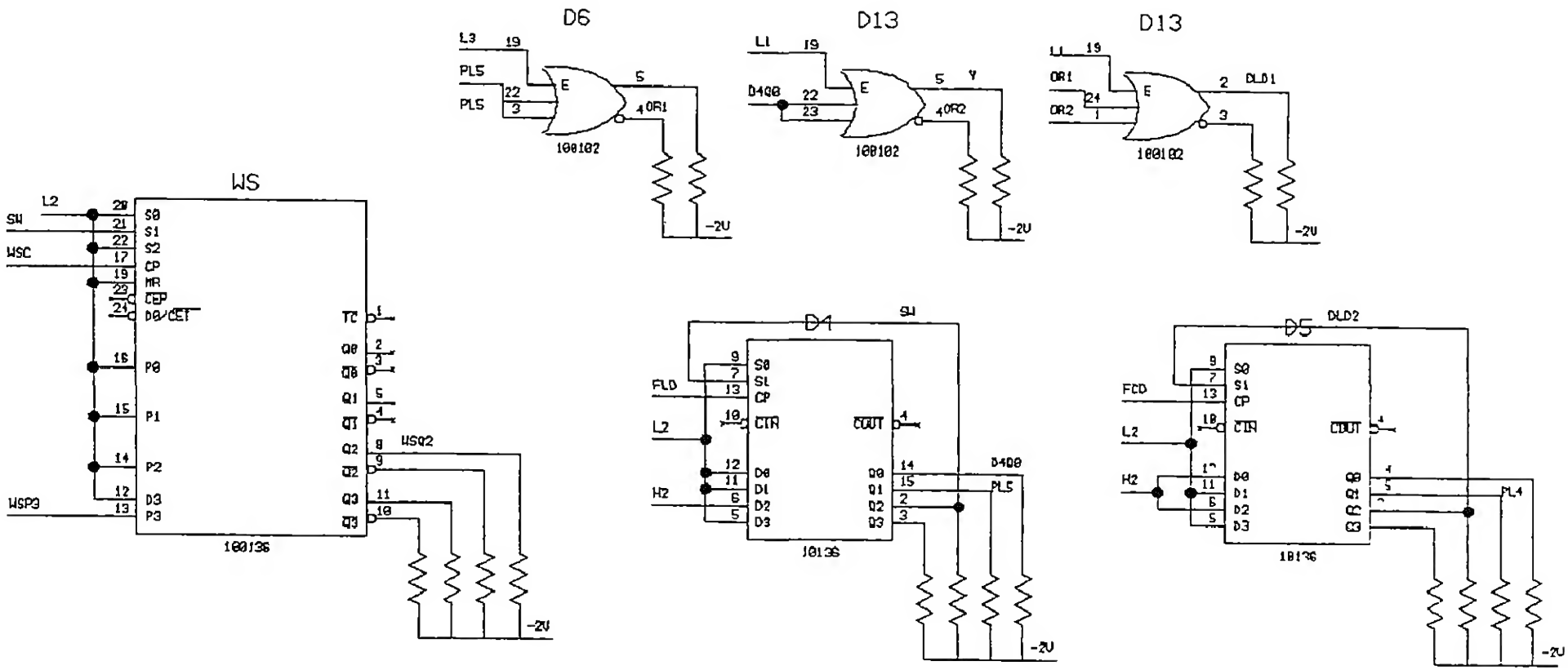


Fig 4 9 The decoder circuit - Part (b)

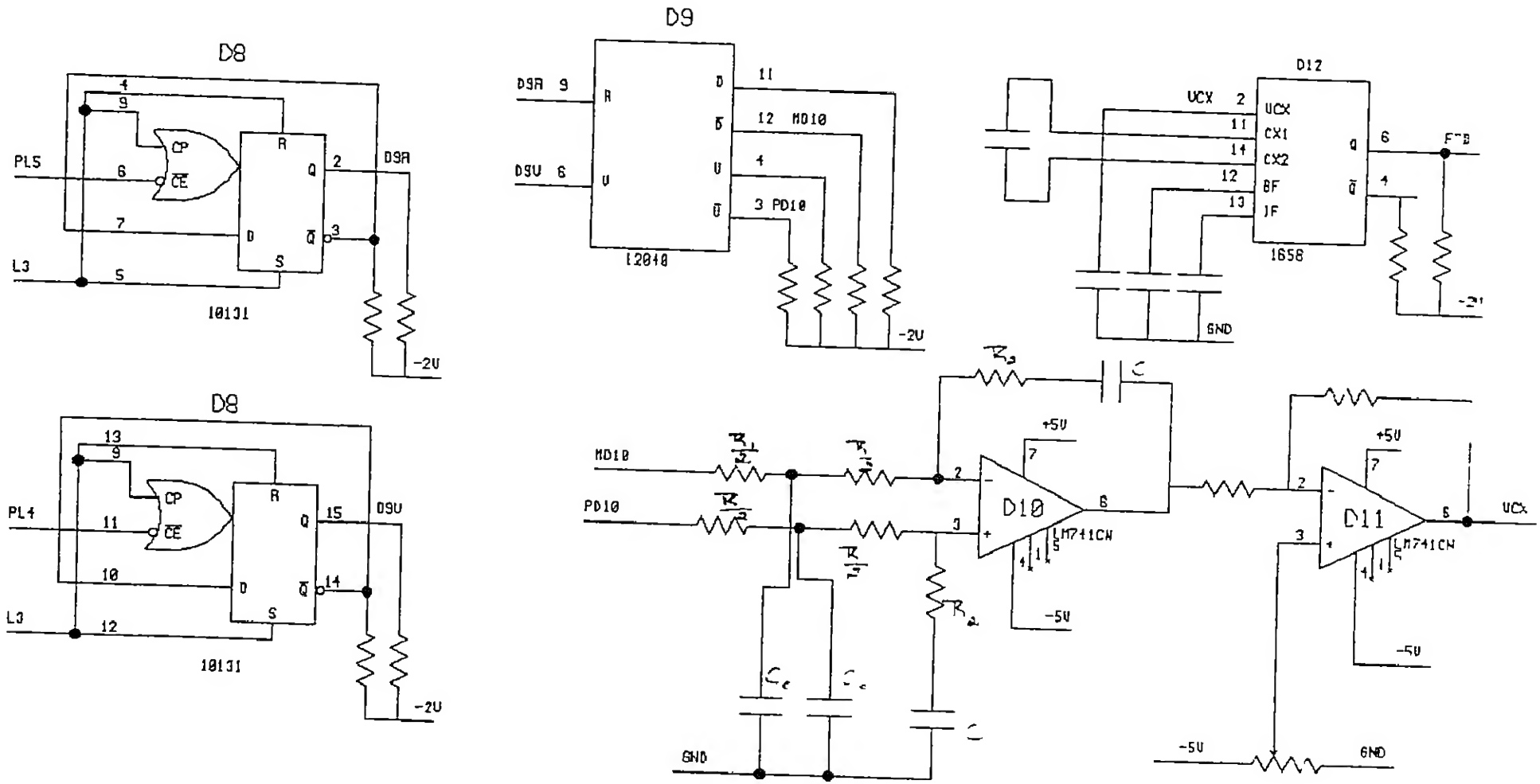


Fig 4.10 The decoder circuit - Part (c)

Figure 4 9 shows the chip 10136 used as a divided-by-five circuit (D4) and a divided-by-four circuit (D5) Also, it shows the chip 100136 used as the word synchronizer (WS) The WS is explained in the next section The divided-by-five function provides the control signals PL5 and DLD1 The chip 10136 (D4) is used as an up-counter by making its So low Q_2 is connected to S_1 and is named as SW The count is started by parallel loading a data $0100_{(2)}$ This data will enable parallel latching to occur once in every five clock pluses For the other four clock periods, this data makes DLD1, Q_2, So, and S_1 high, and the chip is in count-up mode After four clock pulses, the data will become $1000_{(2)}$ Now, in the next four pulses, DLD1 goes low, and again parallel loading of $0100_{(2)}$ data occurs The divided-by-four function is realized by D5 in a similar fashion, with the difference that the parallel data latched in is $0101_{(2)}$ This data enables preset to occur once in every four clock periods in D5

The signal PL4 ($f_{cd}/4$) in the decoder should be synchronized with the signal PL5 ($f_{id}/5$) for the correct operation of the decoder circuit As PL5 does not have a 50% duty cycle, therefore, PL4/2 and PL5/2 are synchronized The chip 10131 is used as a toggle (divided-by-two) flip-flop for both the PL4 and the PL5 signals D8 in Fig 4 10 shows the actual circuit of the divided-by-two operation for the PL4 and the PL5 signals D9 shows the MC12040 chip, which is the phase-frequency detector used D12 is the chip MC1658, which is the voltage-controlled-multivibrator

(VCM) of the PLL. D11 is the level shifting opamp used to level shift the control voltage obtained by the low pass filter so that it lies within the control voltage range of the VCM. The PLL design is given in Section 4.5.2.

4.5.1 THE WORD SYNCHRONIZER

In mB1C coding, the m^{th} and the $(m+1)^{th}$ bits are complementary. This property enables us to separate the five bit coded blocks. Figure 4.11 shows the timing diagram of the word synchronizer (WS). The VCM generated clock is fld. From this, we obtain the line clock in decoder fld by NORing fld with WSQ2 (Q2 output of the word synchronizer). Once in every five fld periods, the m^{th} and the $(m+1)^{th}$ bits are Ex-ORed and the error signal is obtained. Figure 4.8 shows the word synchronizer (WS) chip (100136). The word synchronizer clock (WSC) is a delayed fld clock. The reason for the requirement of this delay is explained in Section 4.5.2.

The divided-by-five (D4) chip generates a SW (word synchronizer) pulse, which goes low once in every five decoder line clock (fld) periods. In this period, the WSP3 pulse is generated. WSP3 is obtained by NORing the error signal and the SW pulse, and is given to P_8 (the most significant parallel input bit of the word synchronizer). WSP3 signal is such that it goes high if an error is detected, and remains low if there is no error. The SW pulse will

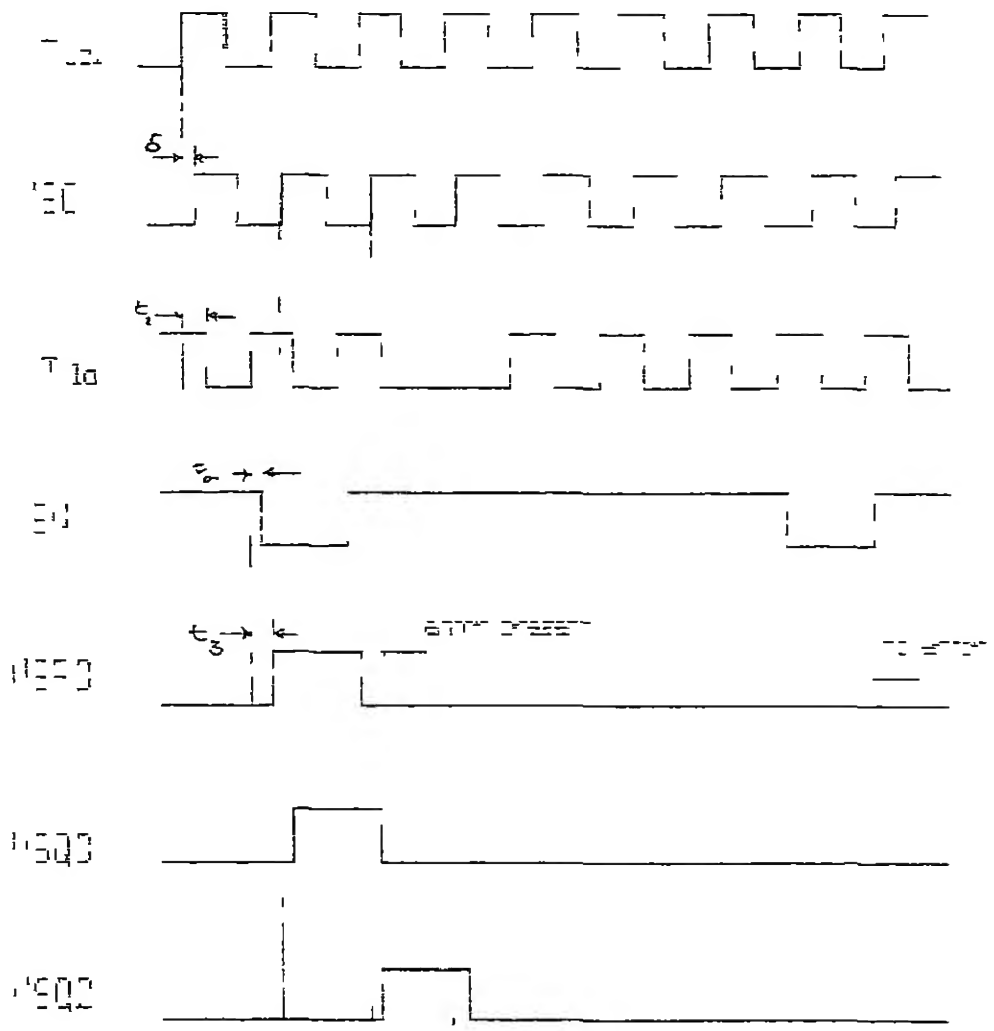


Fig 4.11 The timing diagram of the word synchronizer.

make the word synchronizer chip to act as a parallel latch at the next word synchronizer clock (WSC) When WSC occurs, the error alongwith the data on P_0 to P_2 (which are made low) appear at the output of the word synchronizer (WS) Therefore, the most significant bit of the word synchronizer Q_3 has the error signal If an error occurs Q_3 of the word synchronizer goes high, otherwise it remains low After the next clock, the error is moved to Q_2 of the WS, since, when SW goes high, the WS is in the shift left mode Q_2 of WS will remove a pulse from fld if an error has occurred, otherwise it will remain low thus unaffecting fld

If a pulse is removed from fld, then the next time error will be checked after skipping a data bit, i e , it will check the $(m+1)^{th}$ and the $(m+2)^{th}$ bits Thus, till the correct word is obtained repeatedly, one bit of data will be skipped and the error will be checked at the next SW pulse

4.5 2 THE TIMING CONSTRAINTS IN THE WORD SYNCHRONIZER

The line clock in the decoder fld is generated from fldl by NORing it with Q_2 of the word synchronizer It will have a delay equal to a NOR gate delay represented by t_1, and is approximately equal to 0 75 nsec Figure 4 11 shows the timing diagram of the word synchronizer used SW pulse is generated from fld and it has a delay of t_2 (the delay of D4, i e , the 10136/10137 chip) It is typically 3 3 nsec The error signal WSP3 coming to the word

synchronizer is generated from the SW pulse The delay in the generation of the WSP3 signal is shown by t_g and is given by

$$t_g = \{(t_{D4}) \text{ or } (t_{D1} + t_{XOR})\} + t_{NOR},$$

where, t_{D4} gives the delay in the generation of SW, and$(t_{D1} + t_{XOR})$ gives the delay in generation of the error signal, which includes the delay in D1 to get the m^{th} and the $(m+1)^{th}$ bits, and the delay in the Ex-OR gate respectively The higher of the two delays is to be considered for worst case analysis and it is approximately equal to 4 8 nsec

The timing constraints of the word synchronizer circuit are

1 The SW pulse should be generated before WSC occurs, therefore

$$t_1 + t_2 < (t_{fd}/2) + \delta,$$

where, $t_{fd} = 1/f_{fd}$ and δ is the delay provided to the f_{fdt} signal to generate the word synchronizer clock (WSC) The f_{fd} clock and the word synchronizer clock are both obtained from the f_{fdt} clock recovered by the bit synchronizer The f_{fd} clock aids in obtaining the error signal WSP3 which is latched onto the word synchronizer by the WSC Hence, by delaying the generation of the WSC we make sure that the error is generated before the WSC pulse

2 The error signal WSP3 should appear before the next WSC (word synchronizer clock pulse) This condition is given by

$$t_3 < [(t_{1d}/2) - t_1 + \delta],$$

where, t_1 is the delay due to the NOR gate By making the delay (δ) provided in the generation of WSC equal to t_1, we make the word synchionizei capable of performing upto a frequency which is higher than that obtained without the delay The value of t_3 without the delay is equal to 4 25 nsec, and with a delay of δ equal to t_1, the value of t_3 is equal to $t_{1d}/2$, which is 3 3 nsec, which translates to a value of f_{1d} of 150 MHz

3 However the delay δ provided should not exceed $t_{1d}/2$

4 5 3 THE PLL FREQUENCY SYNTHESIZER DESIGN

The schematic of the PLL frequency synthesizer realized for generating the clock f_{dc} is shown in Fig 4 10 It shows a phase-detector D9, an active low-pass filter D10, and a voltage-controlled multivibrator (VCM) D12 The design of the PLL circuit is the same as that explained in Section 3 5 2 The following design specifications are used for the PLL 1 The phase detector gain is

$$K_d = 0\ 16\ V/rad$$

2 The VCO gain is

$$K_v = 3\ 14 \times 10^8\ rad/sec/V$$

3 N = 2(m) = 8 (for 4B1C coding)

4 The loop gain is

$$K = (K_d K_v/N)\ rad/sec,$$

$= 6.28 \times 10^6$ rad/sec

5 The damping constant δ is chosen to be equal to 0.707, i.e., the system is critically damped

6 The loop bandwidth is selected to be 410 KHz. Hence,

$$\omega_n = 2.58 \times 10^6 \text{ rad/sec now,}$$

$$\tau_1 = R_1C = K/(\omega_n)^2 = 943 \times 10^{-9} \text{ sec,}$$

and

$$\frac{\tau_2}{\tau_1} = \frac{R_2}{R_1} = \frac{2\delta\omega_n}{K} = 0.581$$

6 The spike suppressing capacitor is designed using the following relation

$$10(R_1/2)C_c \geq R_2C$$

From the above relations, we get

$R_1/2 = 4.7$ kΩ,

$R_2 = 5.6$ kΩ,

$C = 100$ pF, and

$C_c = 10$ pF

Some of the important parameters of the PLL are calculated below

1 Lock range

$$f_l = \pm KN/2\pi \text{ MHz,}$$

$$= \pm 8 \text{ MHz}$$

2 Velocity constant

$$K_\gamma = (K_d K_v \tau_2)/\tau_1,$$
$$= 29\ 2 \times 10^6 \text{ rad/sec}$$

3 Capture range

$$f_c = \sqrt{K_\gamma NK}/2\pi \text{ MHz},$$
$$\cong 6\ 1 \text{ MHz}$$

4 Noise bandwidth

$$B_l = (\omega_n/2)\left[\delta + \frac{1}{4\delta}\right] \text{ MHz},$$
$$= 1\ 37 \text{ MHz}$$

5 Acquisition time

$$T_p = \frac{4\ 2\ (\Delta f)^2}{B_l^3} \text{ sec},$$

$$\cong 163\ \mu\text{sec for } \Delta f = 10 \text{ MHz},$$

where Δf indicates the difference in frequency from the center frequency which is to be tracked

The PLL frequency synthesizer is tested, the important parameters are measured, and these are given as follows

1 Lock range +12 MHz to -10 MHz

2 Capture range +11 5 MHz to -9 MHz

4.6 CONCLUSION

In this chapter,the block diagram representation of a decoder circuit alongwith the timing diagram were described Brief description on various types of bit synchronizer was given, followed by the discussion on the design of the bit synchronizer implemented

The decoder circuit was then explained and the word synchronizer was analyzed The PLL frequency synthesizer used in the decoder circuit was given at the end of the chapter

The calculated and the observed values for the performance of the bit synchronizer and the PLL used in the decoder were given The decoder circuit implemented performed satisfactorily upto a frequency of 100 Mbps Beyond which a lot of interference and attenuation in the signal level were observed

CHAPTER 5

SUMMARY AND CONCLUSION

In designing any digital transmission system, selection of the best suitable line code is an important problem In fiber optic digital communication systems, the aim is to achieve the maximum data transmission frequency possible The mB1C code is a simple line coding technique which provides many advantages of line coding, with the addition of just one extra bit and, consequently, with a marginal bandwidth increase Hence, this was chosen for implementation in this work

The details of the coder circuit was given in Chapter 3 By performing a timing analysis of the coder circuit, it was found that the circuit switching speed was limited only by the switching speed of the individual ICs used A PLL frequency synthesizer was used in the coder circuit to generate the line clock f_{lc} from the coder clock f_{cc} These are the two clocks used for clocking the input data and the coded data respectively, in the coder circuit The proper design of printed circuit boards is very important for circuits working at high frequencies A copper clad double-sided PCB with plated-through holes was used in our work The PCB was designed using the PCAD software Placing of the components was done manually, with proper care taken to minimise the effect of stray capacitances and lead inductances during component placement The coder circuit and the PLL were found to work satisfactorily till

100 Mbps, beyond which there was a lot of interference and cross-talk

The details of the decoder circuit was given in Chapter 4 Its performance was similar to that of the coder circuit The timing requirements of the word synchronizer circuit was much more demanding Here again, the circuit performance deteriorated beyond 100 Mbps, however, below 100 Mbps, these circuits performed satisfactorily

The bit synchronizer implemented in this work was of the delay and EX-OR type The NRZ data used did not have a discrete spectral component at the data rate Hence, a delay and EX-OR type of nonlinearity was used for generating a spectral component at the data rate which was tracked by using a PLL It gave good performance with 1010 data streams However, with the PRBS (pseudo-random bit sequence) signals, it was seen to track frequencies only over a very narrow bandwidth This was due to the characteristic of the digital phase-frequency detector used, which was very sensitive to the data transitions

SUGGESTIONS FOR IMPROVEMENT

The performance of the coder and the decoder circuits can be improved by using all 100K ECL chips in the respective circuits In the bit synchronizer PLL, a Gilbert-cell type of multiplier can replace the digital phase-frequency detector By selecting suitable

high frequency discrete components, the PLL can be designed for higher frequencies Due to lack of time, however, not much work could be done in this direction, and it is recommended for future work The voltage-controlled multivibrator chip (MC1658) also has its own frequency limitations Its output is seen to fall below the ECL levels for data rates above 140 Mbps The fall in the amplitude is attributed to the rise time and fall time being larger compared to the total bit interval at higher frequencies Therefore, the design of a discrete component VCO is suggested for future work with due importance given to the rise time and fall time for improved performance In designing PCB s at high frequencies, it is suggested to have all signal lines seperated by ground planes on one layer, while having only the power lines on the other layer The ground planes will provide shielding and reduce the external pickup

Above 100 Mbps, a lot of interference and cross-talk between lines on the PCB were found Also, design of circuits on the PCB is very difficult Therefore, the trend is towards the design of specific purpose ICs (ASICs - application specific ICs) [21] [22] Multigigabit and higher data rate transmission can be obtained by designing monolithic digital circuits employing MESFET and MISFET devices

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APPENDIX A

PHASE LOCKED LOOP (PLL) THEORY

An elementary PLL consists of a phase detector, a loop filter and a VCO, and its linear model is given in Fig A 1 Initial assumptions made before the analysis are

1 the loop is locked, implying that the signal frequency and the VCO frequency are identical,

2 the phase detector is linear, and

3 the phase detector output is proportional to the difference in phase between the two input signals

The notations used in Fig A 1 are

θ_e is the phase error,

θ_i is the phase of the input signal,

θ_o is the phase of the VCO signal,

V_d is the phase detector output,

K_d is the phase detector gain in V/rad,

F(s) is the filter transfer function,

V_c is the controls voltage of the VCO, and

K_o is the VCO gain in rad/sec/V

The closed loop transfer function of the PLL can be obtained [18,19] from Fig A 1 and is given by

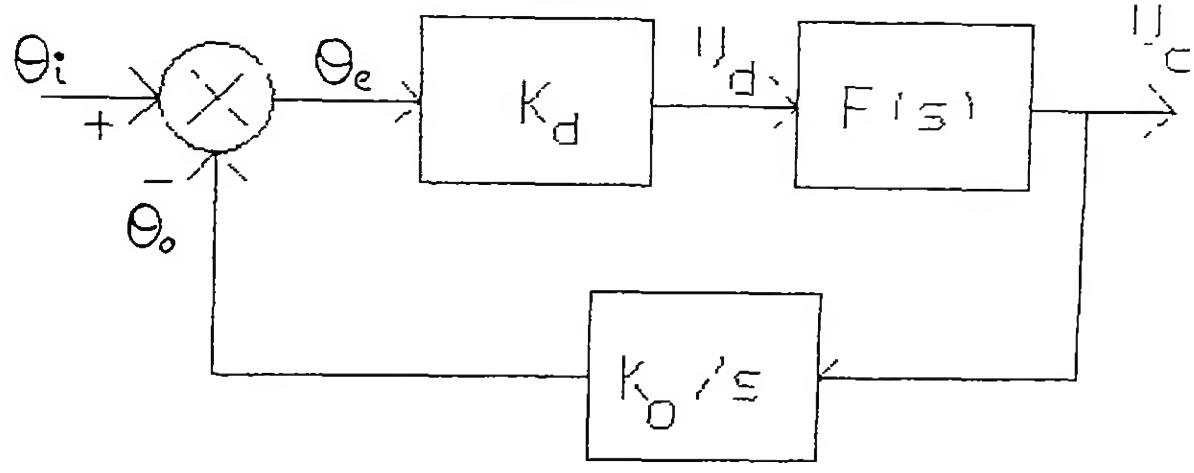


Fig.A.1 The linear model of a PLL.

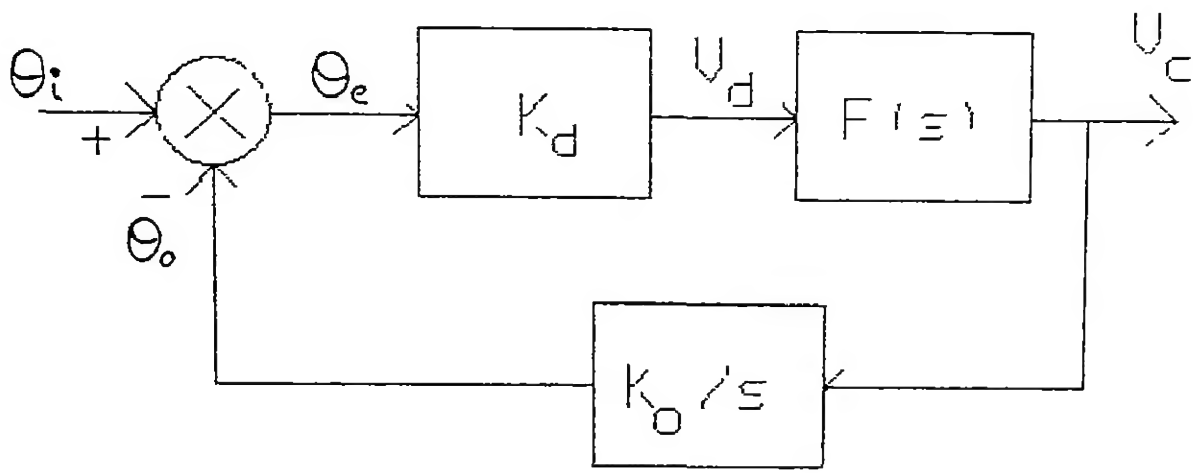


Fig.A.1 The linear model of a PLL.

$$H(s) = \frac{V_c}{\theta_i} = \frac{K_o K_d F(s)}{s + K_o K_d F(s)} \qquad (A\ 1)$$

From Eqn (A 1), it can be seen that F(s) determines the overall closed loop transfer function H(s) exclusively as K_o and K_d are independent of frequency Both active and passive low pass filters can be used as loop filters The passive filter is quite simple and satisfactory for most practical purposes The high dc gain in the case of the active filters improves the tracking performance of the loop Figures A 2 and A 3 show the schematics of the passive and the active filters The filter transfer functions are given by the following expressions

1 For passive filters

$$F_1(s) = \frac{1+s\tau_2}{1+s\tau_1}, \qquad (A\ 2)$$

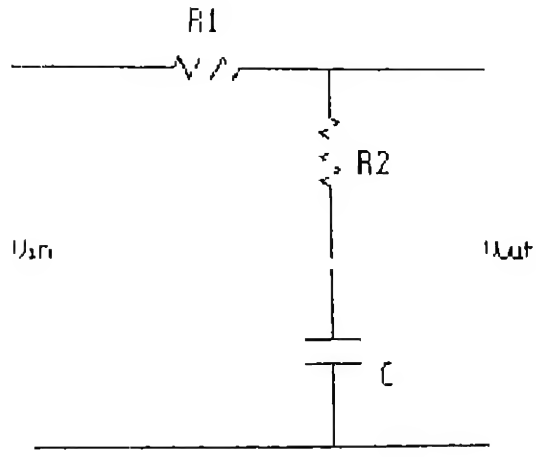
$$\tau_1 = (R_1+R_2)C,$$
$$\tau_2 = R_2C$$

2 For active filters

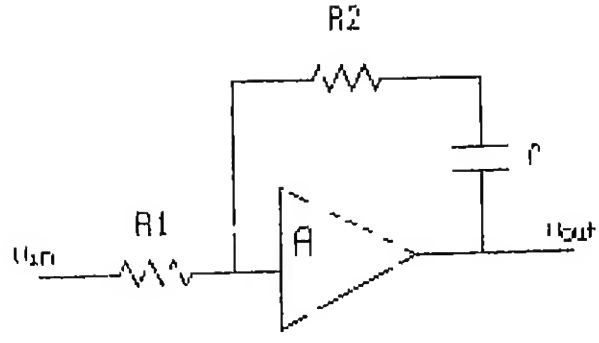
$$F_2(s) = \frac{1+s\tau_2}{s\tau_1}, \qquad (A\ 3)$$

$$\tau_1 = R_1C,$$
$$\tau_2 = R_2C$$

where τ_1 and τ_2 are the time constants associated with the filter



(a)



(b)

Fig.A 2 The schematics of (a) a passive filter

(b) an active filter

Substituting the expression for $F_1(s)$ or $F_2(s)$ in the expression for $H(s)$ as given by Eqn (A 1), we can write the conventional expressions for the closed loop transfer function $H_1(s)$ and $H_2(s)$ for the passive filter and the active filter respectively

1 For passive filters

$$H_1(s) = \frac{s\left[2\delta\omega_n - \frac{\omega_n^2}{K}\right] + \omega_n^2}{s^2 + 2\delta\omega_n s + \omega_n^2}, \qquad (A\ 4)$$

where ω_n is the natural angular frequency of oscillation given by

$$\omega_n^2 = K/\tau_1, \qquad (A\ 5)$$

δ is the damping factor given by

$$\delta = (\omega_n/2)(\tau_2 + \frac{1}{K}), \qquad (A\ 6)$$

and $K = K_o K_d$

2 For active filters

$$H_2(s) = \frac{2\delta\omega_n s + \omega_n^2}{s^2 + 2\delta W_n s + W_n^2}, \qquad (A\ 7)$$

where as before

$$\omega_n^2 = K/\tau_1, \qquad (A\ 8)$$

and

$$\delta = (\omega_n \tau_2)/2 \qquad (A\ 9)$$

LINEAR TRACKING

The PLL can be used for tracking, where it acts as anarrow bandpass filter In bit synchronizers, we use a second order PLL as a tracking filter The linear model for the PLL is used in the analysis done in the previous section, which is true only for small phase errors A small phase error is an indication of good tracking performance The phase error can be obtained from Eqn (A 1) and is given by

$$\theta_e(s) = \frac{s\theta_i(s)}{s + K_o K_d F(s)} \qquad (A\ 10)$$

The phase error consists of two parts, namely the steady-state error and the transient error The steady state error is evaluated using the final value theorem of Laplace transform The common causes for phase error are to a step change in the input phase of magnitude $\Delta\theta$ or an input frequency step $\Delta\omega$ By using the Laplace final value theorem, it is easy to show that the steady-state phase error resulting from a step change in the input phase is zero In other words, the loop will be able to track any

change in the input phase

To measure the phase error, consider the input phase to be a ramp, given by $\theta_i(t) = \Delta\omega t$ The steady state phase error θ_γ obtained from Laplace final value theorem is given by

$$\theta_\gamma = \Delta\omega/K_o K_d F(0) = \Delta\omega/K_\gamma, \qquad (A\ 11)$$

where $K_\gamma = K_o K_d F(0)$ is often called the velocity constant or the DC loop gain K_γ has the dimension of angular frequency given in rad/sec The units of phase detector gain K_d is V/rad when the linear model is assumed, with very small phase error, such that $\sin\theta \cong \theta$ it acts as a multiplier and its units is given in Volts, as $\sin\theta$ is a number Therefore, the units of K_γ is given in rad/sec The incoming frequency almost never matches with the center frequency of the VCO As a result, there is almost always a frequency difference $\Delta\omega$ between the two This results in a steady-state phase error θ_γ which is also termed as the velocity error, the loop stress, or the static phase error

The factor F(0) is contributed by the loop filter Its value for active filters is much larger than for passive filters when actual active filter gain is considered Therefore, loops with active filters will have much better tracking properties than loops with passive filters It will be shown later that a second order loop has another advantage of reducing static phase error and jitter

independently

The transient phase error depends upon the magnitude of the input step, the loop damping factor, and the natural frequency By increasing the loop natural frequency and the damping factor, it is possible to reduce the transient phase error However, this increases the jitter also

In the above discussion, it was assumed that the loop was linear, which implied small phase error The phase error θ_γ is proportional to $\Delta\omega$ As θ_γ increases, the loop goes into nonlinear operation and finally goes out of lock For a sinusoidal phase detector, the phase error is given by the relation

$$\sin\theta_\gamma = \Delta\omega/K_\gamma \qquad \text{(A 12)}$$

Since the magnitude of the sine function cannot exceed unity, for $\Delta\omega$ greater than K_γ, the loop falls out of lock and the phase detector output becomes a beat note, rather than a DC level Hold-in range or lock range $\Delta\omega_h$ of the loop is given by

$$\Delta\omega_h = \pm K_\gamma \qquad \text{(A 13)}$$

This expression states that the lock range can be made arbitrarily large by increasing K_γ However, very high lock range is never reached due to the limitation in the loop filter and the VCO

Many other types of phase detectors have greater linear spans and larger output range, than the sinusoidal phase detectors Hence these offer larger tracking ranges Table A 1 gives the extension factors for different types of phase detectors

TABLE A 1

Extension Factors for different types ofphase detectors

Type	Extension factor
Sinusoidal	1
Triangular	Π/2
Saw Tooth	Π
Sequential Phase/Frequency	2Π

There is some frequency step limit below which the loop does not skip cycles but remains in look, which is denoted as the pullout frequency and labelled $\Delta\omega_{po}$ For values of δ between 0 5 and 1 4, the pullout frequency $\Delta\omega_{po}$ is given by

$$\Delta\omega_{po} = 1\ 8\omega_n(\delta+1) \qquad \text{(A 14)}$$

To reduce the jitter in the timing waveform, it is necessary to keep the static phase error as small as possible In

other words, a second-order loop must be designed for good tracking performance Also, the loop must be designed to have as large DC loop gain as possible

ACQUISITION BEHAVIOR

In all the preceding sections, it was assumed that the loop was already in lock However, a loop starts in an unlocked condition and must be brought into lock either by its own natural actions or with the help of auxiliary circuits The process of bringing the loop into lock is called acquisition If the loop acquires lock by its own natural action, it is called self-acquisition If auxiliary circuits are used for locking, the acquisition is called aided-acquisition

Acquisition is basically a nonlinear phenomenon Under normal circumstances, phase is self acquired When the incoming signal frequency is within a limit, called the lock-in limit to the center frequency of the VCO, the lock takes place without any cycle skipping, but with just a phase transient Though there is no cycle skipping, the loop requires some settling time during which phase transients die out The lock-in limit is approximately given by

$$\text{lock-in limit} \qquad \Delta\omega_L = K \approx K_o K_d F(\infty) \tag{A 15}$$

In the second-order loop, the lock-in range is less than the hold-in or lock range When the initial detuning is greater than $\Delta\omega_l$, the loop starts skipping cycles before locking However, when detuning exceeds another limit $\Delta\omega_p$ (where $\Delta\omega_l < \Delta\omega_p < \Delta\omega_h$) the loop refuses to lock This limit $\Delta\omega_p$ has been called as the capture range or the pull-in range

When the input signal is first applied, the loop is not locked and only a beat note appears at the output of the phase detector Frequency of the beat note slowly decreases with the VCO frequency drifting slowly towards that of the signal, until the lock limit is reached Then the loop snaps into lock without any further cycle skipping The beat note is asymmetric, i e , the negative and the positive portions are unequal, resulting in a net dc value Since a second-order loop has a filter which at least approximates an integrator, a net dc level builds up slowly at the filter output This voltage drives the VCO frequency towards the signal frequency and finally the loop locks, provided that the initial detuning is within the capture range The mathematical analyses required to obtain the capture time and the capture range are quite complicated and also involve some assumptions

The pull-in time T_p is defined as the time required for the average frequency error to change from the initial frequency deviation $\Delta\omega$ to the lock-in limit of $\Delta\omega = K$ It is given by

$$T_p = \frac{(\Delta\omega^2)}{2\delta\omega_n^2} \qquad \text{(A 16)}$$

This expression is valid for $\Delta\omega_l < \Delta\omega < \Delta\omega_p$ For the special case of a high gain second-order loop with $\delta = 0.707$, the pull-in time T_p is given by

$$T_p = \frac{4\ 2(\Delta f)^2}{B^3} \text{ sec}, \qquad \text{(A 17)}$$

where B is the noise bandwidth The largest frequency detuning $\Delta\omega_p$, for which the loop can still pull into lock, is called the pull-in limit and is given by

$$\Delta\omega_p = 2\sqrt{\delta\omega K_\gamma} \text{ rad/sec} \qquad \text{(A 18)}$$

The above expression is valid for sinusoidal phase detectors For phase detectors with extended sawtooth characteristics, $\Delta\omega_l$, and $\Delta\omega_p$ are larger and T_p is smaller Therefore, the quantities calculated using these expressions can be taken as minimum limits for extended phase detectors Pull-in is practical where noise is small, i e , the SNR and the loop bandwidth arelarge enough to permit rapid action, and with simple loop circuits In challenging applications, aided-acquisition is almost always used

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